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Table of Contents

4 SATA Express Connector 5
4.1 SATA Express Connector Overview 5
4.1.1 SATA Express Goals 5
4.1.2 SATA Express Technical Summary 5
4.1.3 SATA Express Scope 7
4.2 SATA Express Signal List 7
4.3 SATA Express Mechanical 11
4.3.1 SATA Express Device Plug Connector 12
4.3.2 SATA Express Device Cable Receptacle Connector 15
4.3.3 SATA Express Host Receptacle Connector 18
4.3.4 SATA Express Host Plug Connector 21
4.3.5 SATA Express Host Cable Receptacle Connector 25
4.3.6 Power Dongle Connector 28
4.3.7 SATA Express Connector Intermateability Summary 31
4.4 SATA Express Connector and Cable Electrical and Mechanical Requirements 32
4.4.1 SATA Express Connector and Cable Assembly Signal Integrity Requirements 32
4.4.2 SATA Express Connector and Cable Shielding Requirements for EMI 32
4.4.3 SATA Express Connector and Cable Assembly DC Electrical Requirements 32
4.4.4 SATA Express Connector and Cable Assembly Mechanical and Environmental Requirements 33
4.5 SATA Express System Electrical Requirements 33
4.5.1 SATA Express AC Coupling Capacitance Requirement 33
4.5.2 SATA Express Interface Detect 34
4.5.3 PCIe Sidebands 37
4.5.4 PCIe Device Power 37
4.6 References and Bibliography 37
4.6.1 References 37
4.6.2 Formal Bibliography 37
4.7 Specification Conventions 37
4.7.1 Definitions 37

4 SATA Express Connector

4.1 SATA Express Connector Overview

SATA Express defines electrical and mechanical requirements for SATA Express, which is a PCI Express (PCIe) connection to the existing standard 3.5 inch and 2.5 inch disk drive form factors for client applications. It is intended for providing a smooth transition path from SATA to PCIe storage, leveraging both PCIe specifications and 3.5 inch and 2.5 inch drive mechanical standards.

4.1.1 SATA Express Goals

SATA Express is developed with the following characteristics:

a) PCIe (see 3.1) connection to client PCIe storage devices;
b) standardized connectors and form factors, fitting in the existing 3.5 inch and 2.5 inch drive mechanical enclosures;
c) muxed PCIe and SATA lanes on the host so the host connector work with either a PCIe or a SATA storage device;
d) both cabling and direct connect solutions to support desktop and notebook product needs; and
e) no PCIe reference clock sent over cable to allow the continued use of the low cost SATA-like cable solutions.

4.1.2 SATA Express Technical Summary

The technical summary of SATA Express is listed below:

a) the focus is on an SATA Express cable and motherboard connector for client applications and a device connector;
b) the form factors supported in SATA Express are SFF-8301 (3.5-inch drive) and SFF-8201 (2.5-inch drive) with no changes;
c) the device connector is based on SFF-8680 with a repurposed pin-out;
d) SATA Express supports x2 PCIe, Gen2 and Gen3, signaling and references PCIe Base and CEM (Card Electromechanical) specifications Rev 3.0 for electrical requirements.
e) SATA Express is compatible with SFF-8639 when server OEMs choose to mux PCIe with SAS/SATA lanes;
f) SATA Express supports legacy SATA devices;
g) PCIe and SATA lanes are muxed on the host so either a SATA or PCIe device operates with the host;
h) SATA Express delivers 5 V and 12 V power to the device with 3.3 V not supported (see 4.5.4); and
i) SATA Express allows existing SATA power supply cable infrastructure be used through the addition of a power supply dongle (see 4.3.6).

The PCIe reference clock (RefClk) is not included in the cabled interface. A separate RefClk with independent SSC (SRIS) architecture is used, similar to the clocking architecture used in SATA.

Figure 1 shows example configurations for SATA Express. In all cases shown, the backward compatibility with SATA is maintained by muxing PCIe and SATA together on the host.

Figure 1 – Example configurations for client

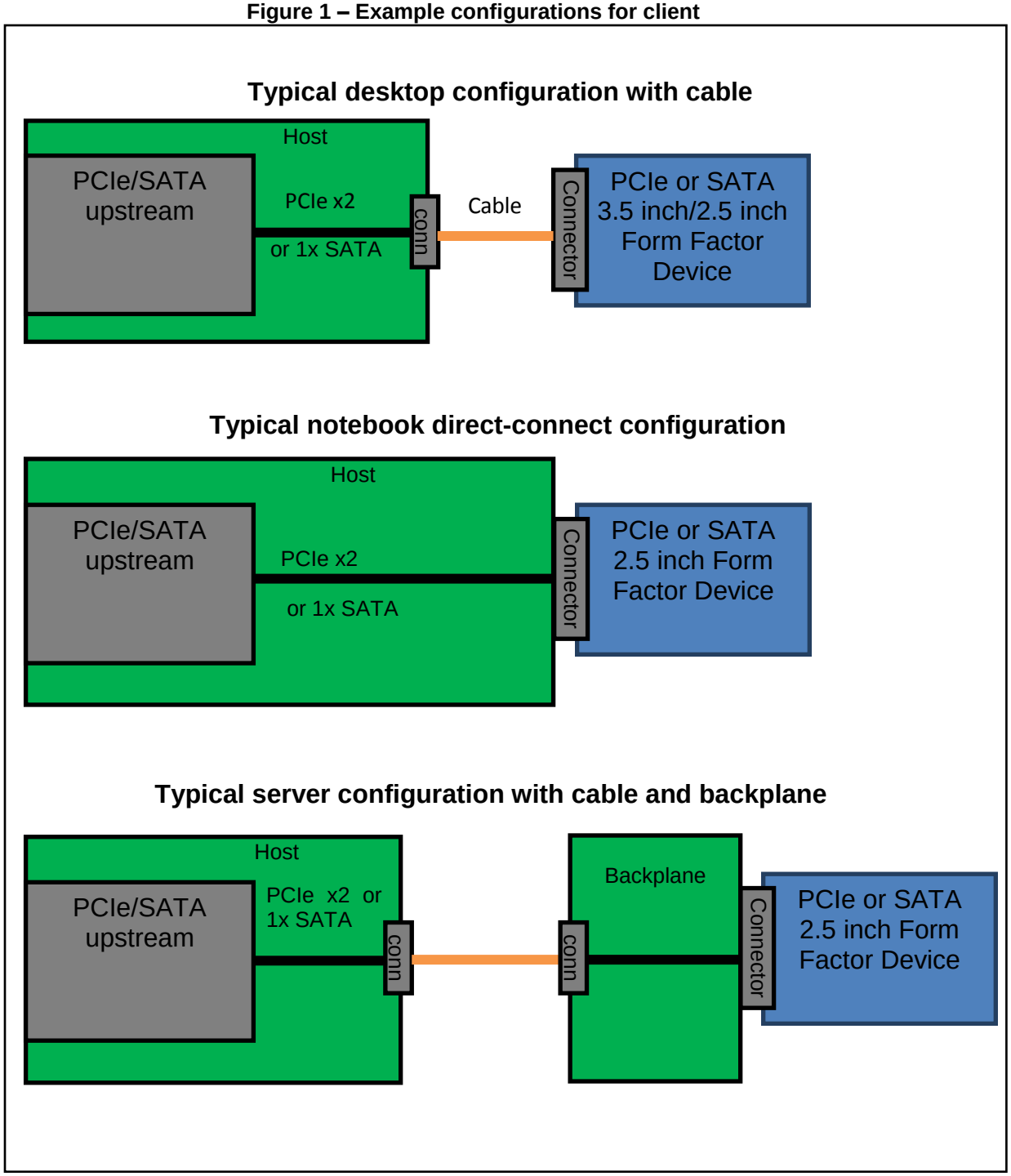


Table 1 summarizes the key characteristics of SATA Express.

Table 1 – Usage Model Summary

Characteristic	Internal 1 m Cabled Host to Device	Direct Connect to Device	Short Backplane to Device
Host-side connector	4.3.4	4.3.3	4.3.3
Device-side connector	4.3.1	4.3.1	4.3.1
Cable length	<= 1 m		
Cable and connector electrical	4.4.1	4.4.1	4.4.1
PCIe Lanes	x2	x2	x2
SATA Lane	SL (single lane) muxed with PCIe	SL (single lane) muxed with PCIe	SL (single lane) muxed with PCIe
PCIe Gen2 [1,2,3]	R	R	R
PCIe Gen3 [1,2,3]	FS	FS	FS
SATA Gen1i and Gen2i	R	R	R
SATA Gen3i	FS	FS	FS

1. The SATA Express cabled topology requires the use of the PCIe PHY that supports SRIS since no RefClk is sent over cable. PCIe PHYs without SRIS capability do not support the cabled application.
2. Optional RefClk pins are provided in the SATA Express host receptacle connector, which allows use of the PCIe PHY that requires common RefClk.
3. System OEM is responsible for the management of PCIe devices with or without common RefClk.

4.1.3 SATA Express Scope

SATA Express is a form factor specification that focuses on connectors and cables for PCIe storage. The connectors on the host are backward compatible extension of SATA connectors. The overall mechanical form factors are compliant with the 3.5 inch and 2.5 inch form factors.

SATA Express defines the following:

a) pin list and signal assignment of the connectors;
b) mechanical definition of the connectors and cable interfaces; and
c) limited electrical specification (largely reference to PCIe and legacy SATA Specifications).

4.2 SATA Express Signal List

The signal list is a combination of SATA and PCIe signals. Table 2 provides an overview of the signals groups. Table 3 gives the complete signal list, usage, and which document governs the signal definition. Most of the signals used in SATA Express are definitively defined in PCIe spec or other sections of this spec (the SATA spec). Figure 2 shows the mapping of signals to the host receptacle connector pins.

Table 2 – Signal List Summary

Usage	Signals	Contacts
x2 PCIe muxed with SATA	2 x (Tx and Rx pairs) + GND pins	14
Power	5 V and 12 V + GND pins	10
Device Activity Signal/Disable Staggered Spinup (optional)	DAS/DSS	1
PCIe CLKREQ# / SATA DEVSLP	CLKREQ#/ DEVSLP	1
PCIe Reset	PERST#	1
PCIe/SATA Interface Detect	IFDet	1
PCIe RefClk (optional)	RefClk+/RefClk- + ClkDet	3
Reserved	Reserved	1
Total		32

Table 3: SATA Express Pin Group (for Host Receptacle and Device Plug Connectors)

Pin Group	Pin Name	Signal Description	Usage	Defining Specification
PCIe/SATA Data	PETp0/A0+, PETn0/A0-	Host transmit PCIe Lane 0/SATA	PCIe/SATA	PCIe/SATA
	PETp1, PETn1	Host transmit PCIe Lane 1	PCIe	PCIe
	PERn0/B0-, PERp0/B0+	Host Receive PCIe Lane 0/SATA	PCIe/SATA	PCIe/SATA
	PERn1, PERp1	Host Receive PCIe Lane 1	PCIe	PCIe
PCIe Reset	PERST#	PCIe Reset	PCIe	PCIe
PCIe RefClk	RefClk+, RefClk-	PCIe common reference clock	PCIe, optional	PCIe
Clock Detect	ClkDet	Detect device PCIe clock type	PCIe	SATA
L1 PM Substate / Dev Sleep	CLKREQ#/DEVSLP	PCIe: Enter/exit L1 PM substate SATA: Enter/exit device sleep	PCIe/SATA	PCIe/SATA
PCIe/SATA Detect	IFDet	Detect a PCIe drive	PCIe/SATA	SATA
SATA Sideband (optional)	DAS/DSS	Device Activity Signal / Disable Staggered Spinup	SATA	SATA
Reserved	Reserved	Reserved for future use	Reserved	
Power	12 V	12 V power	PCIe/SATA	SATA
	5 V	5 V power	PCIe/SATA	SATA
	GND	Ground return	PCIe/SATA	SATA

Figure 2 – SATA Express Pinout Table for Host Receptacle and Device Plug Connectors

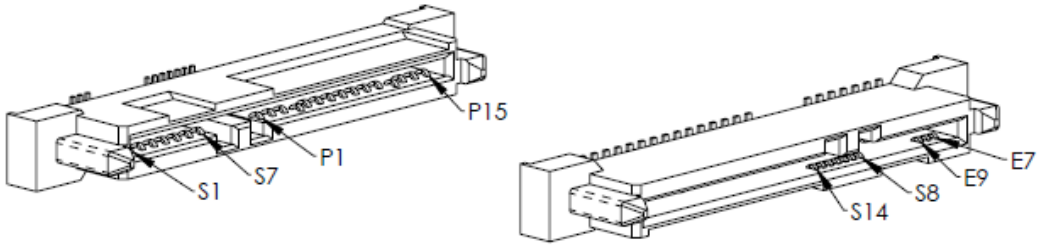


Table 4 – SATA Express Pin List for Host Receptacle and Device Plug Connectors

Pin #	Name[1]	Signal Description[1]	Usage	Signal Direction	Mating Sequence[9]
S1	GND	Ground	PCIe/SATA		2nd
S2	PETp0/A+	PCIe Lane 0 Host Tx / SATA Tx pair[2]	PCIe/SATA	Host Output	3rd
S3	PETn0/A-				
S4	GND	Ground	PCIe/SATA		2nd
S5	PERn0/B-	PCIe Lane 0 Host Rx / SATA Rx pair[2]	PCIe/SATA	Input to Host	3rd
S6	PERp0/B+				
S7	GND	Ground	PCIe/SATA		2nd
S8	GND	Ground	PCIe only		2nd
S9	PETp1	PCIe Lane 1 Host Tx pair	PCIe only	Host Output	3rd
S10	PETn1				
S11	GND	Ground	PCIe only		2nd
S12	PERn1	PCIe Lane 1 Host Rx pair	PCIe only	Input to Host	3rd
S13	PERp1				
S14	GND	Ground	PCIe only		2nd
P1	Reserved[4]	Reserved for future use	PCIe/SATA		3rd
P2	PERST#[4]	PCIe reset	PCIe only	Host Output	3rd
P3	CLKREQ#/DEVSLP[4]	L1 PM substate / Device sleep	PCIe/SATA	Host Output	2nd
P4	IFDet[5]	Interface (PCIe/SATA) detect	PCIe/SATA	Input to Host	1st
P5	GND	Ground	PCIe/SATA		2nd
P6	GND	Ground	PCIe/SATA		2nd
P7	V5[3]	5 V power, pre-charge	PCIe/SATA	Host Output	2nd
P8	V5[3]	5 V power	PCIe/SATA	Host Output	3rd
P9	V5[3]	5 V power	PCIe/SATA	Host Output	3rd
P10	GND	Ground	PCIe/SATA		2nd
P11	DAS/DSS	Device Activity Signal / Disable Staggered Spinup	SATA only	Bi-Dir	3rd
P12	GND	Ground	PCIe/SATA		1st
P13	V12[3]	12 V power, pre-charge	PCIe/SATA	Host Output	2nd
P14	V12[3]	12 V power	PCIe/SATA	Host Output	3rd
P15	V12[3]	12 V power	PCIe/SATA	Host Output	3rd
E7	RefClk+[7]	PCIe common RefClk	PCIe only, optional [6]	Host Output	3rd
E8	RefClk-[7]				
E9	ClkDet[8]	PCIe RefClk detect	PCIe only, optional [6]	Input to Host	2nd

Figure 5 Notes:

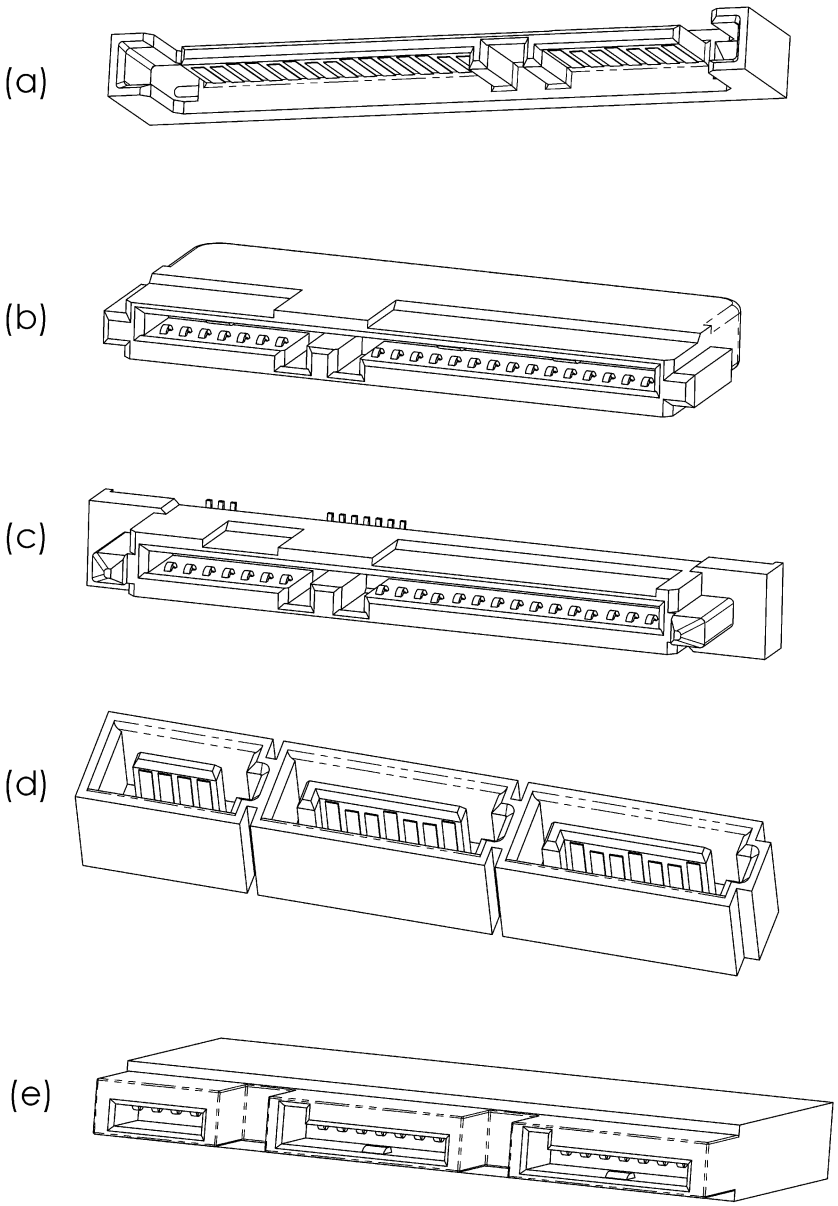
1. The "Name" and "Signal Description" columns are relative to the host, as defined by each protocol specification.
2. Muxing of the PCIe and SATA lanes is required for the host. Only the PCIe Lane 0 is required to mux with the SATA lane for the host receptacle connector since the client SATA device has only a single lane. For the host plug connector, both PCIe lanes (0 and 1) shall be muxed with SATA. This allows connections to two separate SATA devices via independent cables.
3. The power pins on the PCIe device shall be bused together for each supply voltage, in the same way as defined in the legacy SATA specification.
4. Pins P1 to P3 were defined as the 3.3 V pins in previous revisions of this Specification (i.e., SATA rev 3.1) and have since been retired. They are repurposed to be PERST# and other signals in SATA Express. To avoid damage to a PCIe device, the components that connect to those pins shall be able to tolerate the application of 3.3 V.
5. Pin P4 is a GND in previous revisions of this specification (i.e., SATA rev 3.1). It is named IFDet for interface detect in SATA Express. The detail interface detect mechanism is discussed in 4.5.2.
6. The RefClk pins E7 and E8 are defined following SFF-8639. Support of the common RefClk is optional. Management of system compatibility with PCIe devices requiring the common RefClk is beyond the scope of SATA Express.
7. For cabled applications, there is no reference clock (RefClk) included in the host cable plug connector (see 4.3.4), requiring an SRIS architecture. Requirements associated with the separate RefClk with independent SSC are defined in the PCIe Base Specification 3.0 ECN- Separate RefClk Independent SSC Architecture.
8. ClkDet (i.e., pin E9) is used by the host to detect the device RefClk type. If a SATA Express device requires the common RefClk, then the device shall ground pin E9. If a SATA Express device supports SRIS, then the device shall not ground pin E9.
9. Mating sequence defined here is for the host receptacle connector and device plug connector. The mating sequence for the cabled case is defined in 4.3.4.

4.3 SATA Express Mechanical

The following SATA Express connectors are defined, as illustrated in Figure 3:

a) device plug connector;
b) device cable receptacle connector;
c) host receptacle connector;
d) host plug connector; and
e) host cable receptacle connector.

Figure 3 – Illustration of SATA Express Connectors



4.3.1 SATA Express Device Plug Connector

The SATA Express device plug connector is physically similar to the standard SAS device connector defined in SFF-8680. The cable retention feature requirements are unchanged, the

keying is different, and optional pins are added (i.e., E7, E8, and E9) for applications requiring RefClk. The SATA Express device plug connector mates with:

a) SATA Express host receptacle connector;
b) SATA Express device cable receptacle connector;
c) SFF-8639 backplane connector; and
d) SFF-8482, SFF-8630, and SFF-8680 SAS receptacle connectors.

Management of the non-interoperability issues regarding mating the SATA Express device plug connector to SAS receptacles is beyond the scope of SATA Express.

Figure 4 shows an isometric view of the SATA Express device plug connector and Figure 5 defines the SATA Express device plug connector mating interface.

Figure 4 – SATA Express Device Plug Connector Isometric Drawing

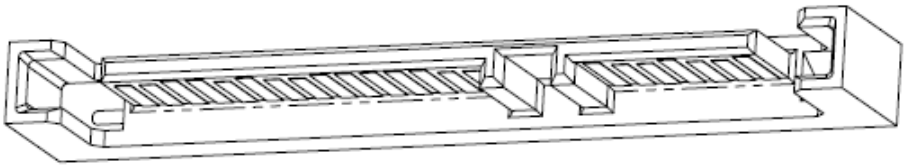


Figure 5 – SATA Express Device Plug Connector Drawing (part 1 of 2)

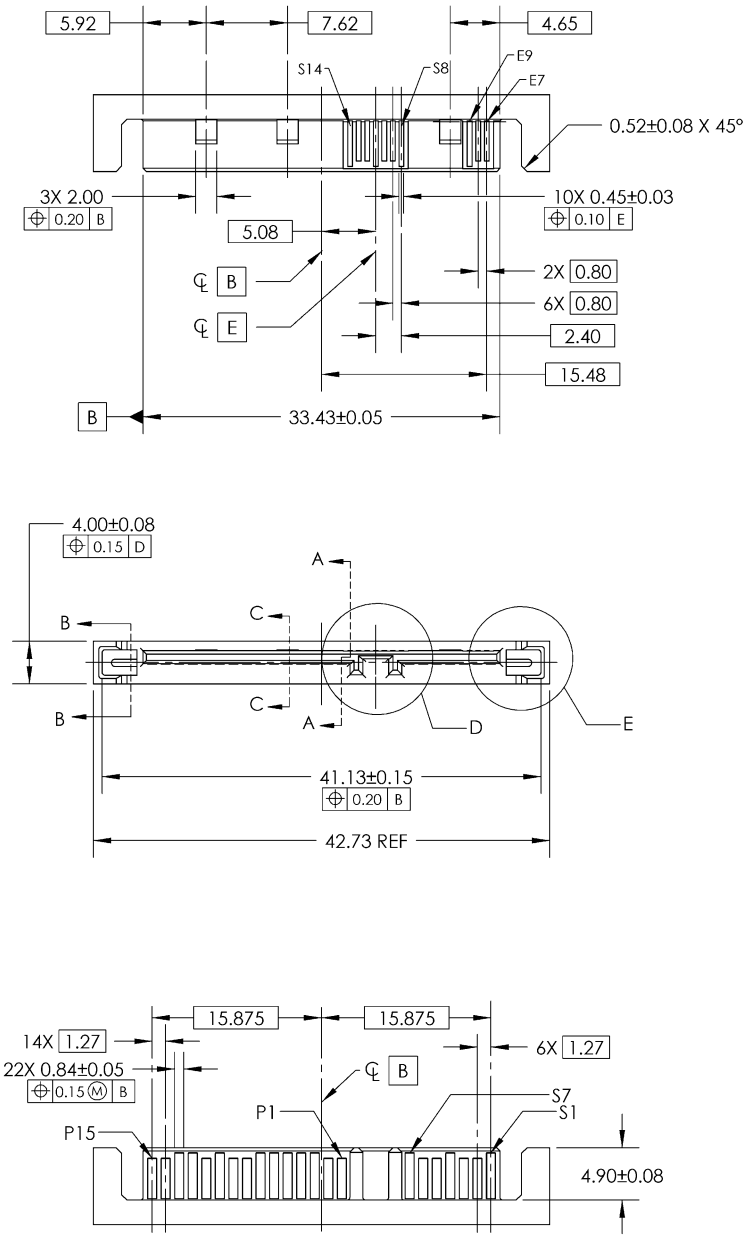
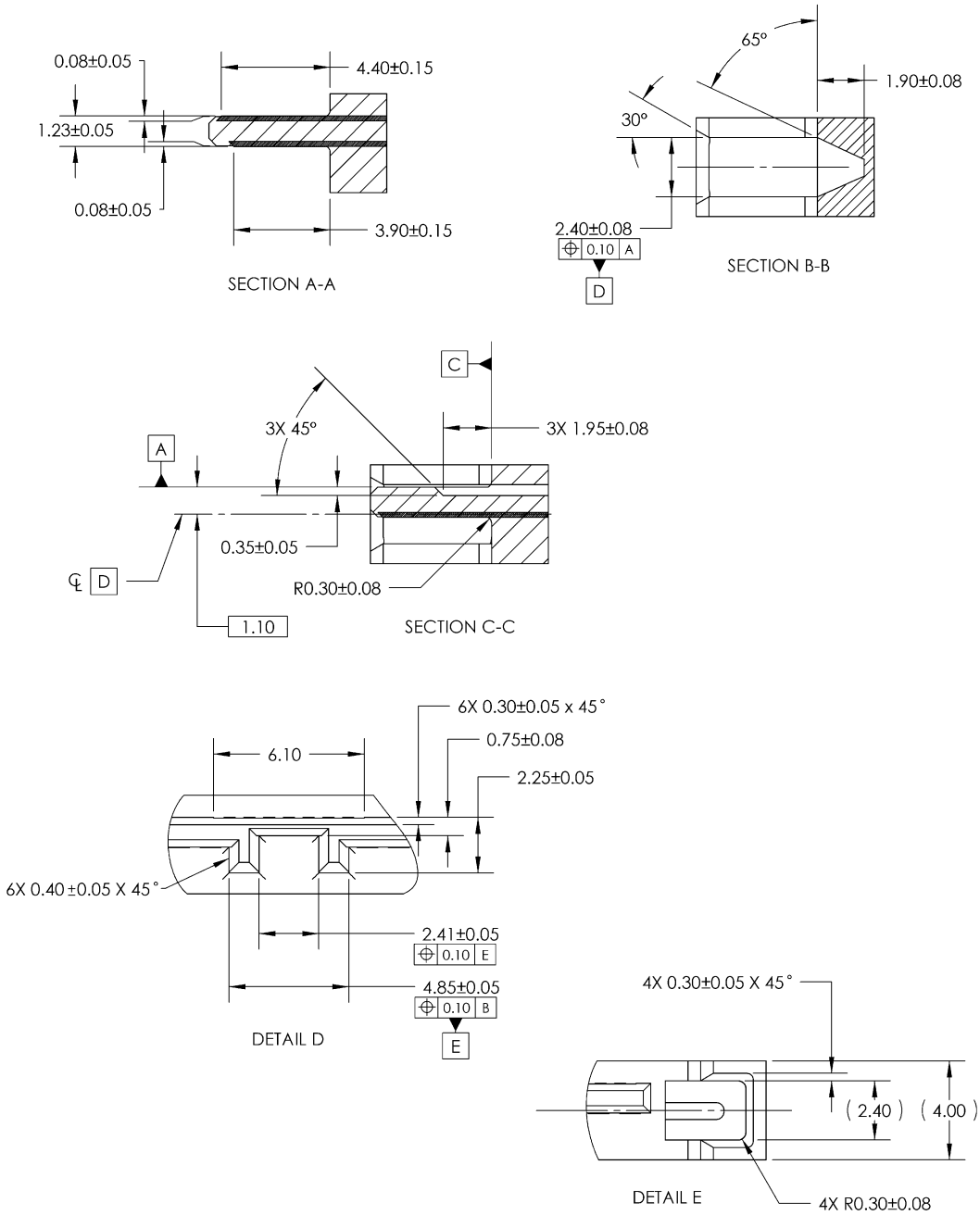


Figure 5 – SATA Express Device Plug Connector Drawingn (part 2 of 2)

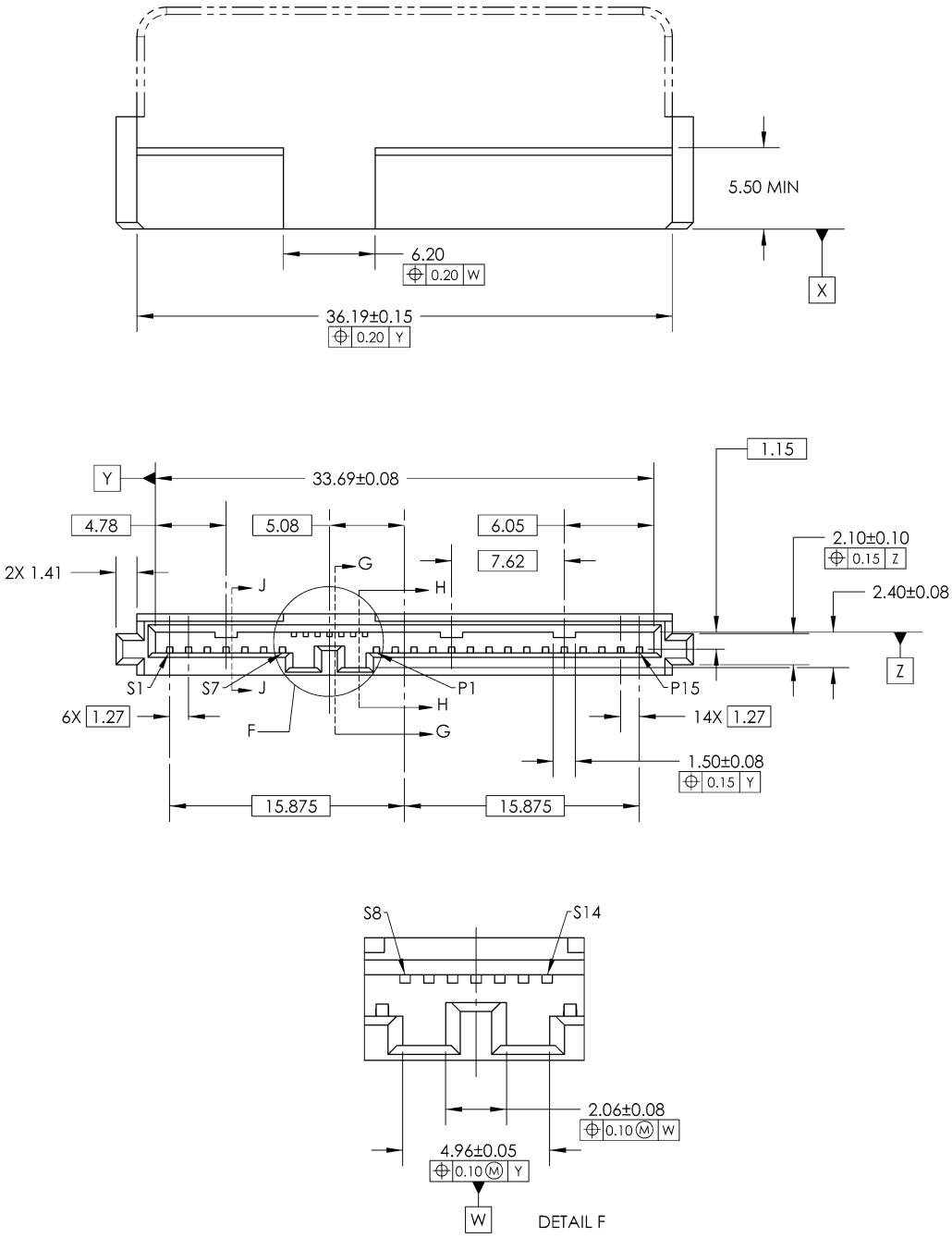


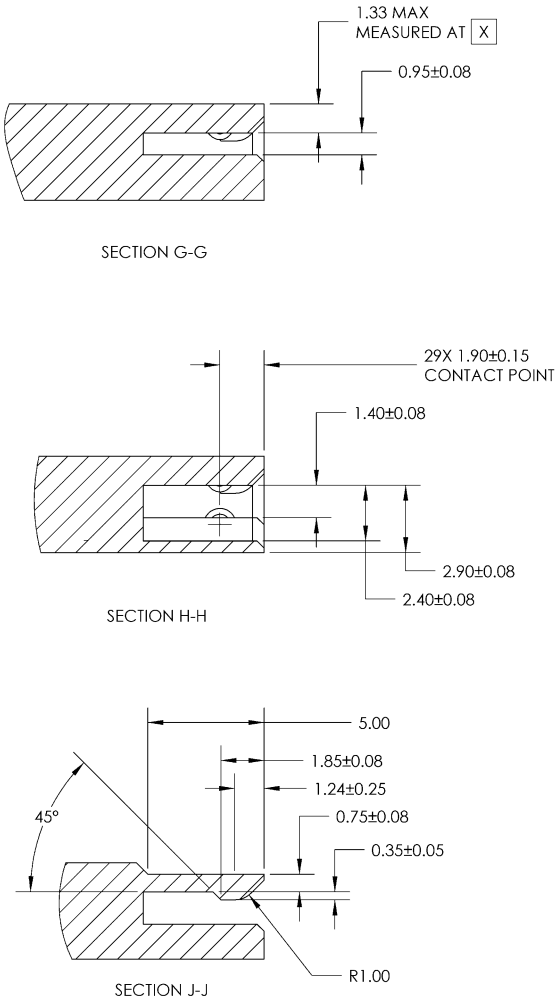
4.3.2 SATA Express Device Cable Receptacle Connector

The SATA Express device cable receptacle connector mates with the SATA Express device plug connector or the SATA device plug connector. It is physically similar to the SAS backplane

connector defined in SFF-8680, but has a different pin definition. The SATA Express device cable receptacle connector is keyed to prevent insertion of a SAS drive plug. Figure 6 defines the mating interface of the SATA Express device cable receptacle connector. RefClk is not supported in cabled applications since E7, E8, and E9 are not included in this connector.

Figure 6 – SATA Express Device Cable Receptacle Connector Drawing





4.3.3 SATA Express Host Receptacle Connector

The SATA Express host receptacle connector is identical to SATA Express device cable receptacle connector except for the following differences:

a) the SATA Express host receptacle connector may include optional contacts E7, E8, and E9 for RefClk support; and
b) the SATA Express host receptacle connector has no retention features (see View Section J-J in Figure 6).

The SATA Express host receptacle connector mates with the following connectors:

a) SATA Express device plug connector; and
b) SATA device plug connector.

Figure 7 shows an isometric view of the SATA Express host receptacle connector and Figure 8 defines the SATA Express host receptacle connector mating interface. Note that Figure 8 does not include all the necessary dimensions or section views to complete the interface definition. Refer to Figure 6 for completeness.

Figure 7 – SATA Express Host Receptacle Connector Isometric Drawing

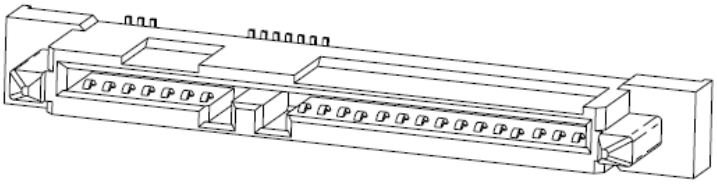


Figure 8 – SATA Express Host Receptacle Connector Drawing (part 1 of 2)

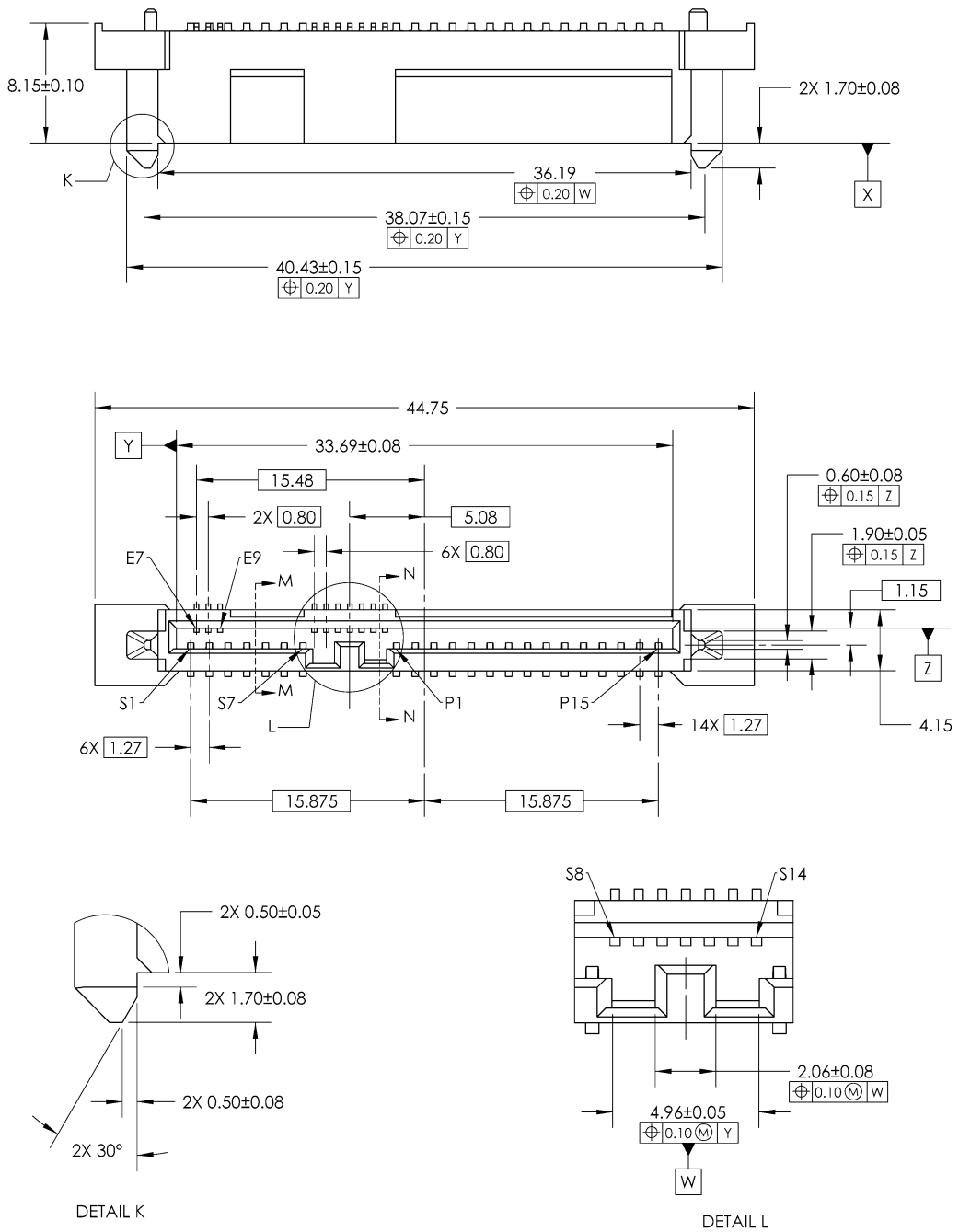
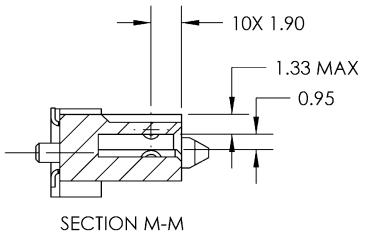
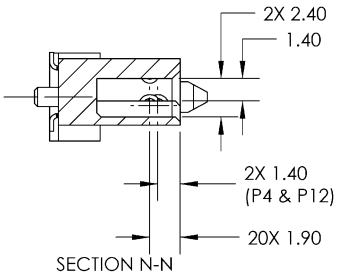


Figure 8 – SATA Express Host Receptacle Connector Drawing (part 2 of 2)





4.3.4 SATA Express Host Plug Connector

The SATA Express host plug connector may be considered an extension of the SATA host plug connector. Figure 9 illustrates the SATA Express host plug connector. It is essentially two SATA host plug connectors joined together, plus an additional section for sidebands.

The SATA Express host plug connector mates with the following connectors:

a) the SATA Express host cable receptacle connector; and
b) the SATA single lane cable receptacle connector.

The pinout of the host plug connector in isometric view is shown in Figure 9 and the pinout table is given in Table 5. It contains only a subset of the pins listed in Table 4. The reserved pin shall be NC (i.e. no connect) on the host, cable and device.

Table 6 shows the SATA Express cable wire connection. Figure 10 and Figure 11 are the SATA Express host plug connector mechanical drawings.

Figure 9 – SATA Express Host Plug Connector Pinout (Isometric View)

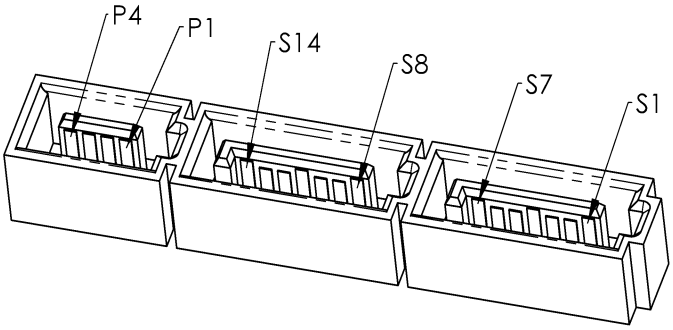


Table 5 – SATA Express Host Plug Connector Pin List

Pin #	Name	Signal Description	Usage	Signal Direction	Mating
S1	GND	Ground	PCIe/SATA		1st
S2	PETp0/A0+	PCIe Lane 0 Tx / SATA Port 0 Tx pair	PCIe/SATA	Host Output	2nd
S3	PETn0/A0-				
S4	GND	Ground	PCIe/SATA		1st
S5	PERn0/B0-	PCIe Lane 0 Rx / SATA Port 0 Rx pair	PCIe/SATA	Input to Host	2nd
S6	PERp0/B0+				
S7	GND	Ground	PCIe/SATA		1st
S8	GND	Ground	PCIe/SATA		1st
S9	PETp1/A1+	PCIe Lane 1 Tx /SATA Port 1 Tx pair	PCIe/SATA	Host Output	2nd
S10	PETn1/A1-				
S11	GND	Ground	PCIe/SATA		1st
S12	PERn1/B1-	PCIe Lane 1 Rx /SATA Port 1 Rx pair	PCIe/SATA	Input to Host	2nd
S13	PERp1/B1+				
S14	GND	Ground	PCIe/SATA		1st
P1	Reserved	Reserved for future use	PCIe/SATA		2nd
P2	PERST#	PCIe reset	PCIe only	Host Output	2nd
P3	CLKREQ#/ DEVSLP	PCIe L1 PM Substate / SATA device sleep	PCIe/SATA		2nd
P4	IFDet	Interface detect	PCIe/SATA	Input to Host	1st

Table 6 – SATA Express Cable Wire Connection

Host Cable Receptacle Connector		Wire	Device Cable Receptacle Connector	
Pin #	**Name**		**Name**	**Pin #**
S1	GND	Drain wire	GND	S1
S2	PETp0/A0+	Shielded differential pair	PETp0/A0+	S2
S3	PETn0/A0-		PETn0/A0-	S3
S4	GND	Drain Wire	GND	S4
S5	PERn0/B0-	Shielded differential pair	PERn0/B0-	S5
S6	PERp0/B0+		PERp0/B0+	S6
S7	GND	Drain wire	GND	S7
S8	GND	Drain wire	GND	S8
S9	PETp1	Shielded differential pair	PETp1	S9
S10	PETn1		PETn1	S10
S11	GND	Drain wire	GND	S11
S12	PERn1	Shielded differential pair	PERp1	S12
S13	PERp1		PERn1	S13
S14	GND	Drain wire	GND	S14
P1	Reserved		Reserved	P1
P2	PERST#	Discrete wire	PERST#	P2
P3	CLKREQ#/ DEVSLP	Discrete wire	CLKREQ#/ DEVSLP	P3
P4	IFDet	Discrete wire	IFDet	P4

Figure 10 – SATA Express Host Plug Connector Isometric Drawing

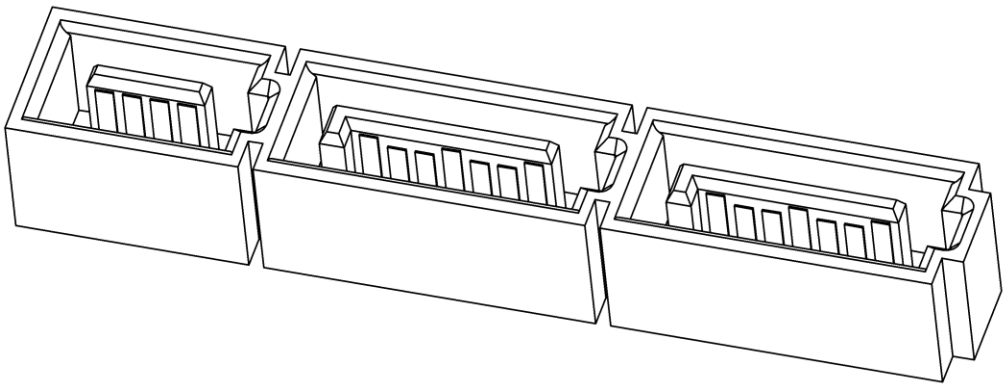
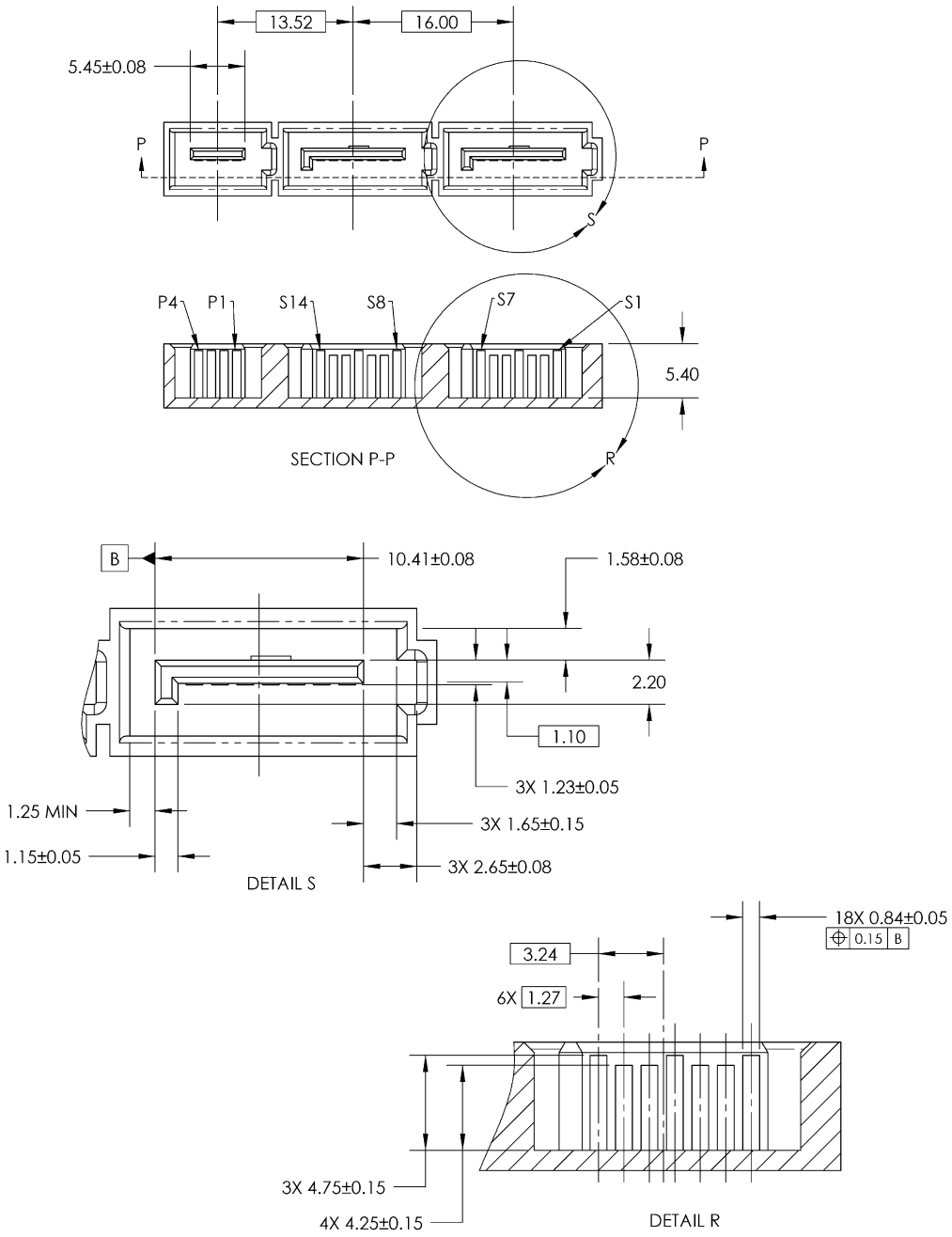


Figure 11 – SATA Express Host Plug Connector Drawing



4.3.5 SATA Express Host Cable Receptacle Connector

The SATA Express host cable receptacle connector mates with only the SATA Express host plug connector. Figure 12 shows an isometric view of the SATA Express host cable receptacle connector. Figure 13 defines the mating interface of the connector. It may be considered an extension of the SATA signal cable receptacle connector.

The following descriptions apply to Figure 13:

a) power is not delivered through the cable; and
b) the cable retention solution is similar to SATA (i.e., both friction lock and metal latches may be used).

Figure 12 – SATA Express Host Cable Receptacle Connector Isometric Drawing

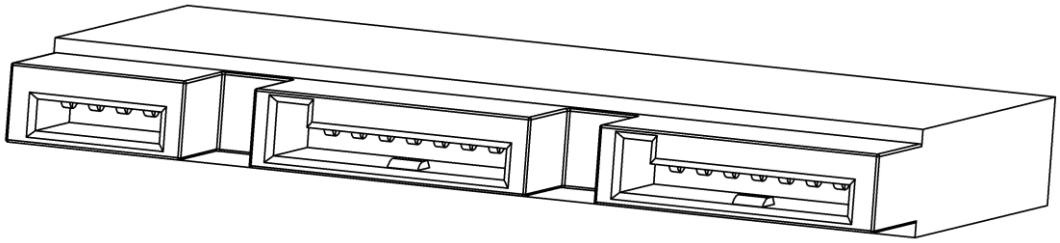


Figure 13 – SATA Express Host Cable Receptacle Connector Drawing (part 1 of 2)

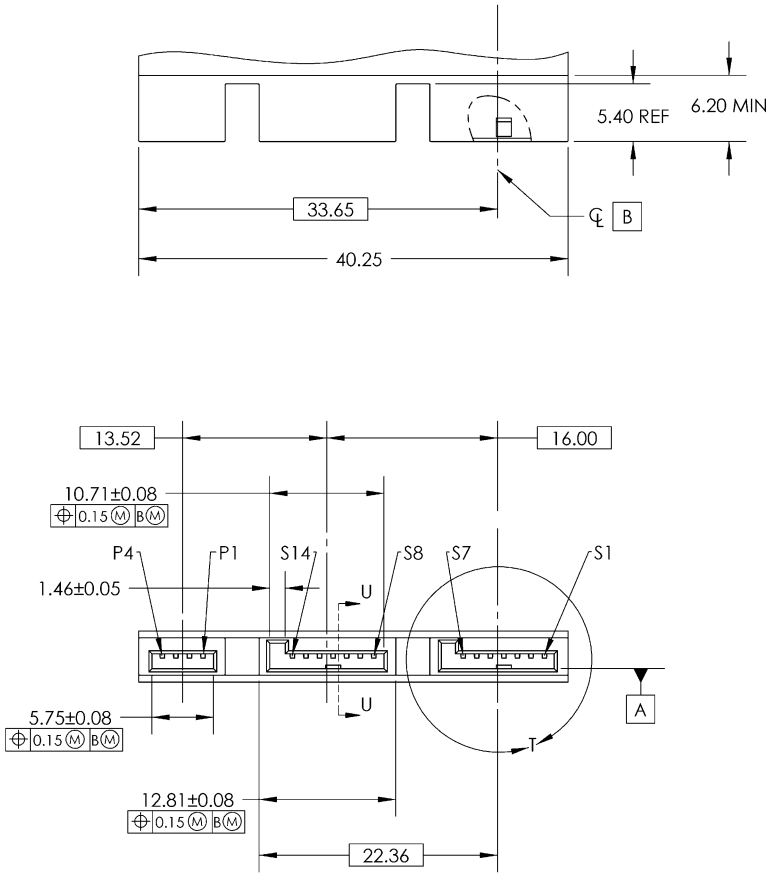
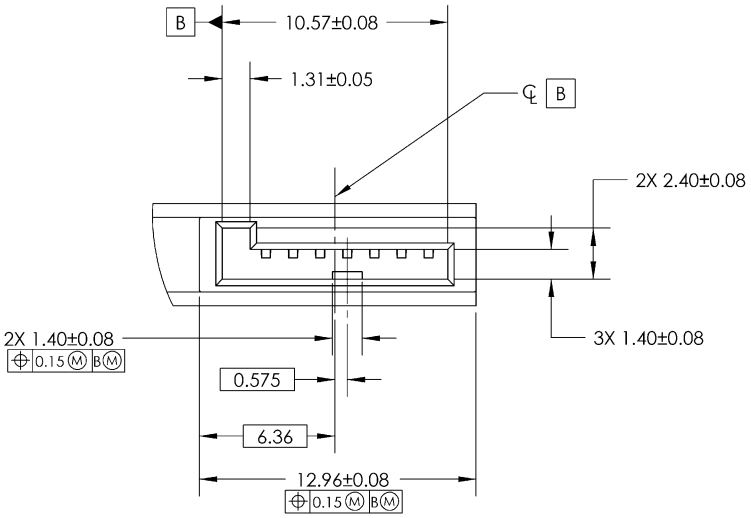
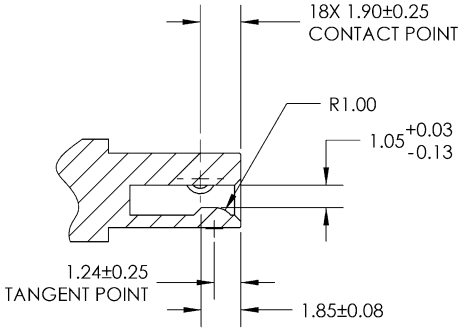


Figure 13 – SATA Express Host Cable Receptacle Connector Drawing (part 2 of 2)



DETAIL T

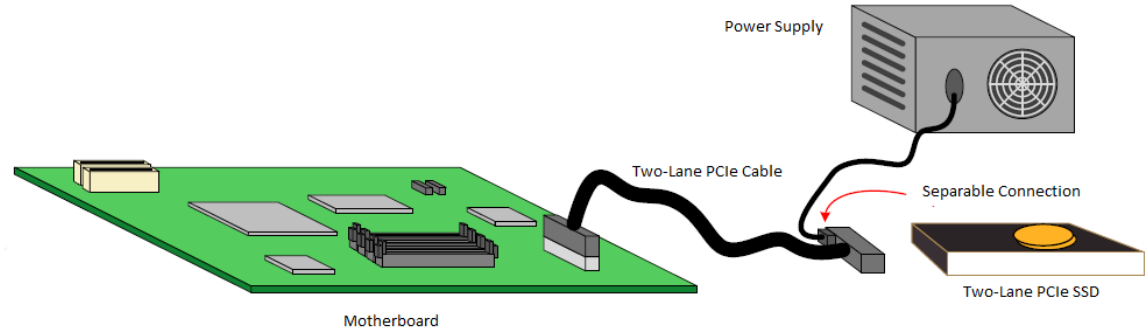


SECTION U-U

4.3.6 Power Dongle Connector

To allow the coexistence of SATA and SATA Express, reuse of the existing power supply infrastructure is desired in many usage models. The SATA Express device cable receptacle connector defined in 4.3.2 supports two PCIe lanes and power. This is different from SATA, which allows two separate connectors, one for signal and one for power, to plug into the device plug connector. To enable use of the standard SATA power cable receptacle connector with the SATA Express device cable receptacle connector, a power dongle is needed, as illustrated in Figure 14.

Figure 2 – Illustration of Power Dongle Usage



Implementation of the power dongle on the SATA Express device cable receptacle connector is vendor specific. The example in Figure 15 allows the standard 15 pin SATA power cable receptacle connector to mate directly to the SATA Express device cable receptacle connector. The example in Figure 16 provides a pigtail power dongle from the SATA Express device cable receptacle connector. Implementation is not limited to the configurations illustrated in these two examples.

Figure 3 – Example Power Dongle To be Used with the 15 pin SATA Power Connector

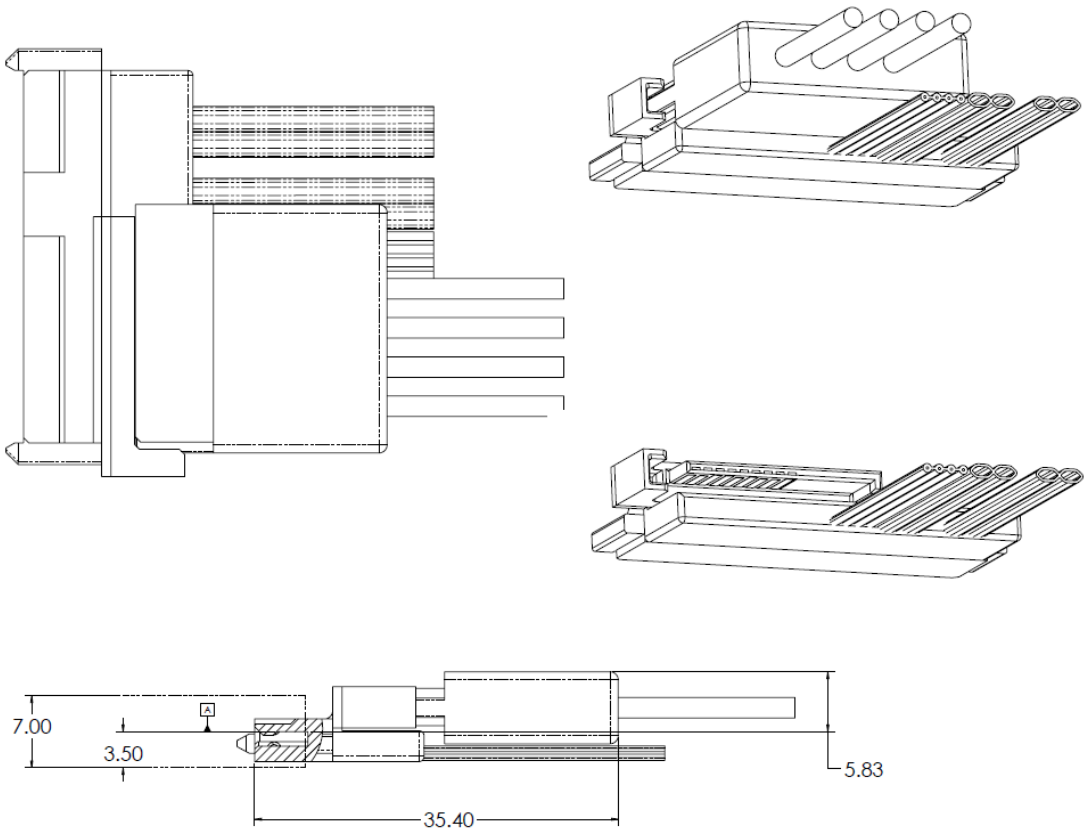
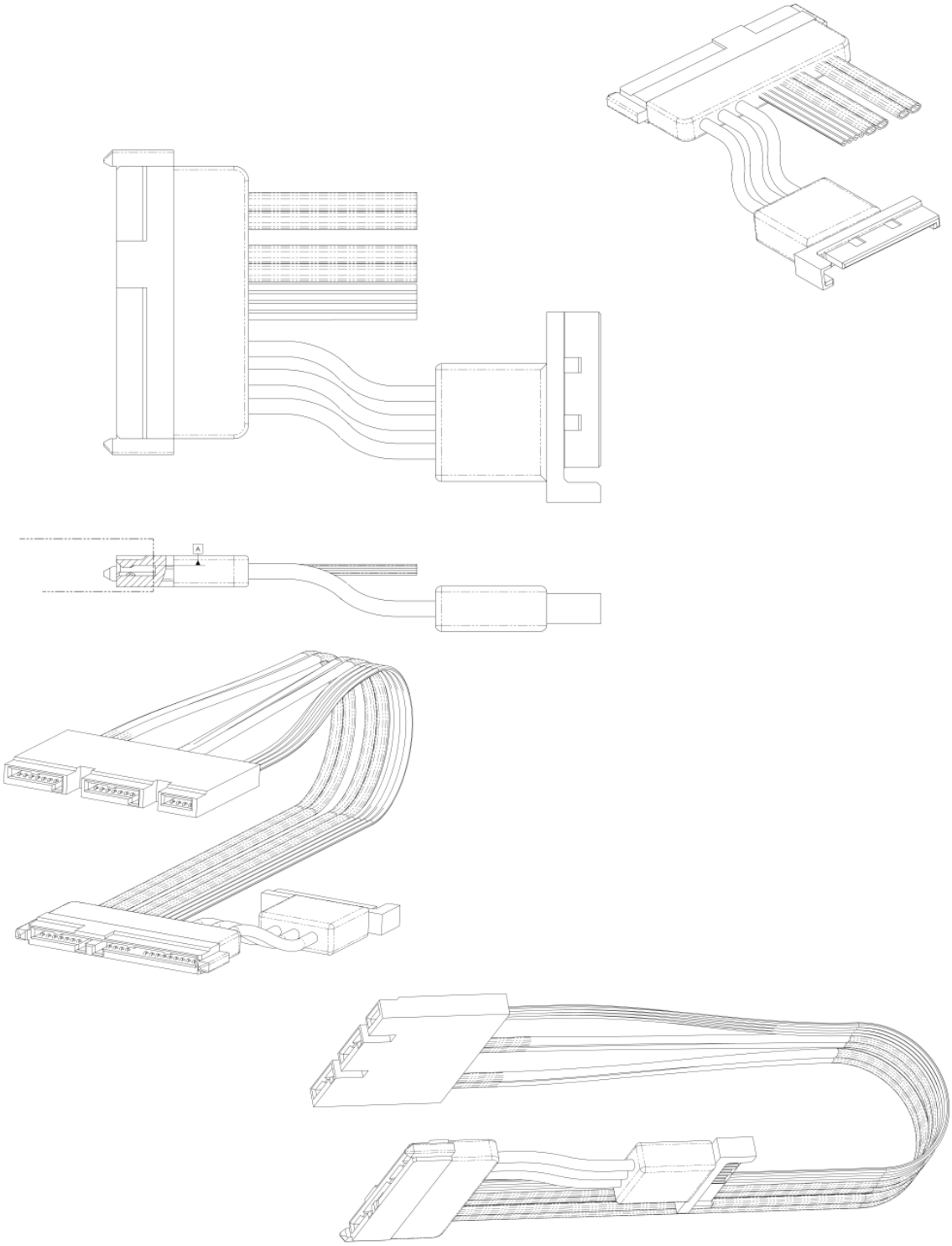


Figure 4 – Example Power Pigtail To be Used with the 15-pin Power Connector



4.3.7 SATA Express Connector Intermateability Summary

The connector intermatability summary is provided in Table 7 for each of the connectors defined in SATA Express.

Table 7 – Connector Intermatability Summary

Connector	Intermateable with
SATA Express Host Receptacle Connector	SATA Express device plug connector (SATA spec) [1] SATA device plug connector (SATA spec) [1]
SATA Express Device Plug Connector	SATA Express host receptacle connector (SATA spec) [1] SFF-8639 backplane receptacle connector [2] SATA Express device cable receptacle connector (SATA spec) [1] SAS/SAS MultiLink backplane and cable receptacle connector [3]
SATA Express Host Plug Connector	SATA Express host cable receptacle connector (SATA spec) [1] 7-pin SATA single lane cable receptacle connector(s) [1]
SATA Express Host Cable Receptacle Connector	SATA Express host plug connector (SATA spec) [1]
SATA Express Device Cable Receptacle Connector	SATA Express device plug connector (SATA Spec) [1] SATA Device Plug Connector (SATA spec)[1]
Power Dongle (on the backside of the SATA Express device cable receptacle connector)	SATA power cable receptacle connector (SATA spec) [1]

[1] Interface is supported.
[2] Interface is supported if muxing of SATA/SAS/PCIe are implemented in SFF-8639 host.
[3] Interface support is beyond the scope of this specification.

4.4 SATA Express Connector and Cable Electrical and Mechanical Requirements

SATA Express electrical requirements shall conform to the PCI Express Specifications. SATA Express cabled applications require the PCIe PHY that supports SRIS.

SATA Express covers only the necessary electrical and mechanical requirements in order for connector and cable manufacturers to make SATA Express cables and connectors. It includes the connector and cable assembly signal integrity requirements. References are provided if requirements are defined in other standards.

4.4.1 SATA Express Connector and Cable Assembly Signal Integrity Requirements

To ensure interoperability of the connectors and cable assemblies, the signal integrity requirements shall conform to PCIe CEM (Card Electromechanical Spec) connector spec, but with modification to the differential insertion loss and intra-pair skew requirements.

The mated cable assembly includes the raw cable plus two mated connectors on both ends of the cable. It is required that the mated cable assembly have a differential insertion loss not exceeding -4.2 dB to 4 GHz and -10.0 dB to 6 GHz. In addition, the insertion loss curve should be free of resonance up to 4.5 GHz.

The mated cable assembly shall have a different intra-pair skew ≤ 10 ps, as measured with a differential Time Domain Transmission (TDT) (risetime=50 ps, measured from the 20 % threshold to 80 % threshold). The delays from each line of the pair are measured at the 50 % voltage crossing, and the delay difference from the two lines is reported as the intra-pair skew.

Note

Connector PCB footprint is one of the major sources of impedance mismatches, mainly from the parasitic of a through-hole (TH) or SMT pad. The recommendations are provided to minimize connector PCB launch mismatches:

a) TH a relatively small finished hole size of 0.61 mm (24 mil) is recommended with appropriate pad and anti-pad sizes (e.g., a 0.91 mm (36 mil) pad and a 1.52 mm (60 mil) differential anti-pad); and
b) SMT a small pad that meets DFM (design for manufacturability) rules should be used. The ground plane immediately underneath the signal pads should be voided to remove excessive parasitic.

The cable wire termination area is another major source of impedance mismatches. Careful wire management with minimum cable shield and dielectric strip-off is recommended.

4.4.2 SATA Express Connector and Cable Shielding Requirements for EMI

Since RefClk is not present on the cable with the SRIS architecture, there is no additional connector or cable shielding requirements beyond what is done for the SATA connector and cable. System designers should pay particular attention to RFI (Radio Frequency Interference), avoiding the placement of the SATA Express cable near wireless radios since this may cause RFI issues.

4.4.3 SATA Express Connector and Cable Assembly DC Electrical Requirements

The connector and cable assembly DC electrical requirements are the same as those specified for other SATA connectors in this specification.

4.4.4 SATA Express Connector and Cable Assembly Mechanical and Environmental Requirements

The connector and cable assembly mechanical and environmental requirements are the same as those specified for other SATA connectors in this specification.

4.5 SATA Express System Electrical Requirements

The SATA Express system electrical requirements cover:

a) AC coupling capacitance;
b) PCIe sidebands; and
c) power.

Most electrical characteristics that are defined as part of other standards, particularly PCIe, are referenced, rather than defined in SATA Express.

4.5.1 SATA Express AC Coupling Capacitance Requirement

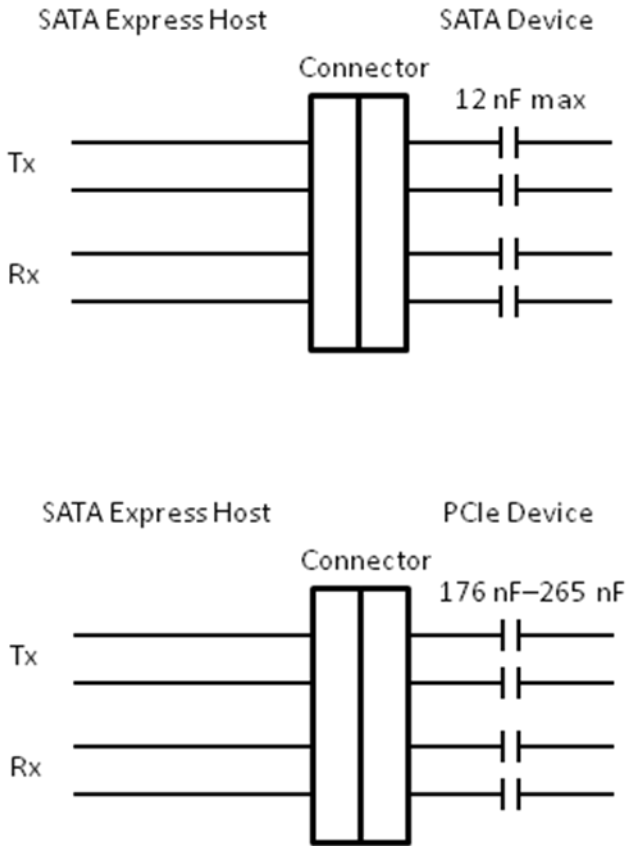
PCIe and SATA have different AC coupling capacitance requirements:

a) PCIe Gen1 and Gen2 – min 75 nF, max 265 nF, Tx side only;
b) PCIe Gen3 – min 176 nF, max 265 nF, Tx side only; or
c) SATA – max 12 nF, both Tx and Rx sides (except for DC coupled Gen1i).

The following AC coupling cap is required for SATA Express:

a) there shall be no AC coupling capacitor placed on the SATA Express host, as illustrated in Figure 18; and
b) the PCIe device shall have AC coupling capacitors on both the Tx and Rx lanes, as shown in Figure 18. The capacitance value shall be 176 nF min to 265 nF max, as defined in the PCIe spec.

Figure 18 – AC Coupling Cap Requirements

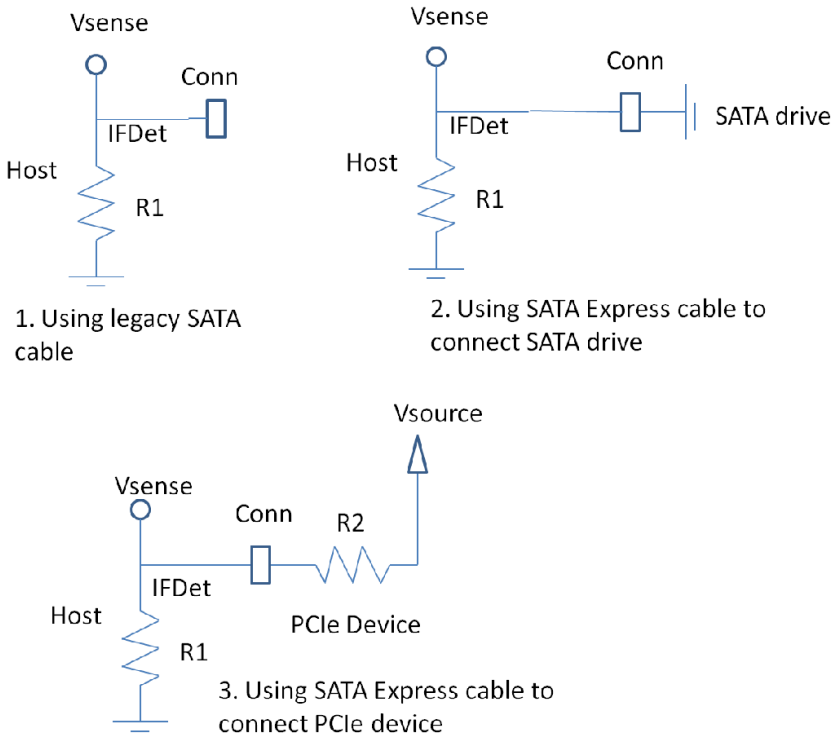


Such AC coupling cap requirements meet both the SATA and PCIe AC cap specifications. In the case of a SATA device working with a SATA Express host, a 12 nF max cap is provided by the SATA drive. A SATA Express host does not support SATA Gen1 DC coupled devices.

4.5.2 SATA Express Interface Detect

An interface detect (IFDet) is defined to detect if the device plugged in is SATA or PCIe. Figure 19 illustrates the interface detect mechanism for the cabled case.

Figure 19: Interface Detect Mechanism



To make this mechanism work, a pull-down resistor R1 is required on the host and a pull-up resistor R2 is needed on the PCIe device, connecting to voltage source Vsource. IFDet is always shorted to GND for SATA drives, but when using a legacy SATA cable the host IFDet will be open requiring the host to apply the pull-down as illustrated in Figure 19.

Table 8 summarizes the logic states for Vsense for various cases.

Table 8 – Logic States of Vsense

Usage case	Vsense	Device type detected
SATA cable with SATA drive	Low	SATA
SATA Express cable with SATA drive	Low	SATA
SATA Express cable with PCIe drive	High	PCIe
SATA drive in SATA Express host receptacle connector	Low	SATA

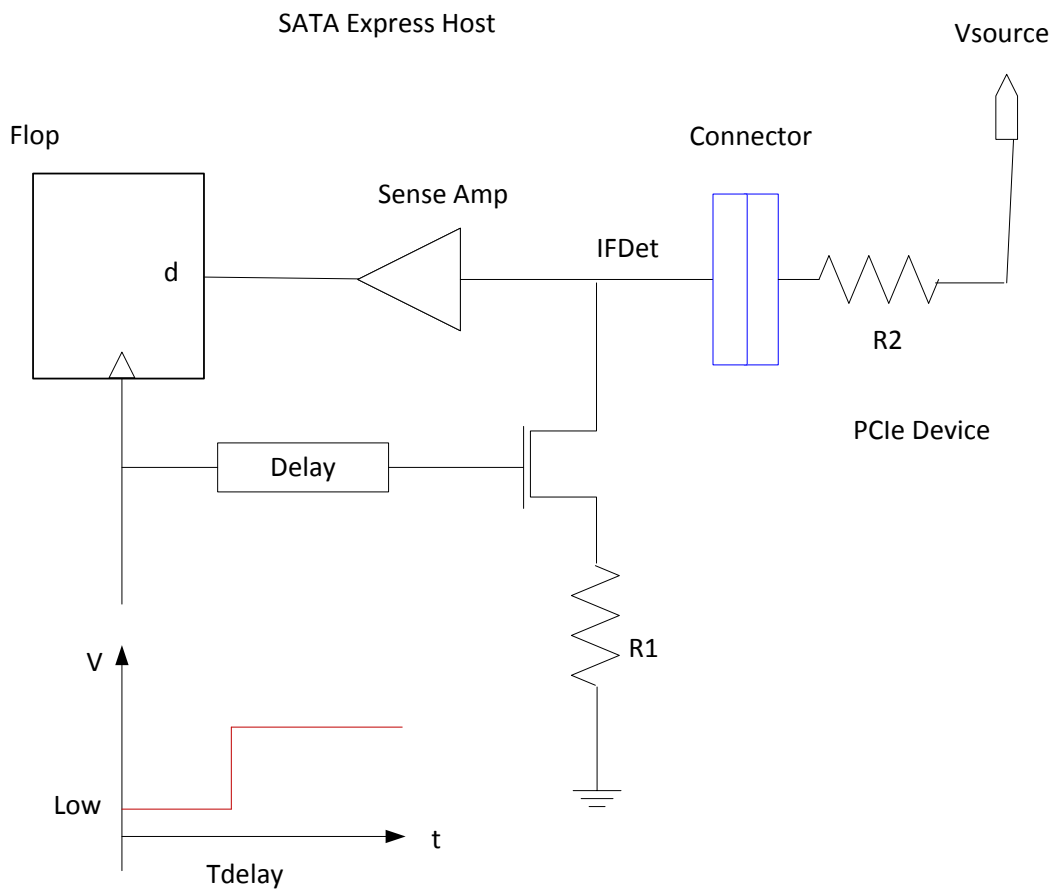
PCIe drive in SATA Express host receptacle connector	High	PCIe

The followings are the requirements to support the interface detect:

a) the pull-down resistor R1 on the host may be on-die or discrete. The value of R1 shall be 20 kohm with a relative tolerance of +/- 40 %;
b) the pull-up resistor R2 on the PCIe device of 5 kohm with a relative tolerance of +/- 10 % shall be used, connecting to the 1.8 V rail with a relative tolerance of +/-5 %; and
c) the SATA Express cable shall have a wire to connect the IFDet pins at both ends.

Note
To prevent DC drain when a PCIe device is connected to the SATA Express host, a switch may be implemented on host to shut down the DC drain path when detection is completed, as illustrated in Figure 20. The host/controller allows Tdelay amount of time for V_{sense} to stabilize. Then it latches in the detected voltage and opens the DC path to ground thus avoiding a constant DC power drain.

Figure 20: Interface Detect, Shutting Down DC Path after Detection



4.5.3 PCIe Sidebands

The PCIe reset, PERST#, is a required PCIe sideband. Its electrical requirements are given in the PCIe CEM Specification 3.0.

CLKREQ# is also required for a PCIe device to enter/exit the L1 PM substate. See PCIe Base Specification 3.0 for detail.

If the RefClk is not included in the SATA Express cabled interface, system manufacturers shall ensure that the PCIe receivers used for SATA Express cabling as discussed in this specification support the SRIS capability, as specified in the PCIe Base Specification 3.0 ECN - Separate Refclk Independent SSC Architecture.

4.5.4 PCIe Device Power

PCIe devices get their power on 12 V or 5 V. 12 V shall be provided for the host systems that use the 3.5 inch drives. For systems that support only the 2.5 inch drives, 5 V shall be provided.

4.6 References and Bibliography

4.6.1 References

PCI Express® Specifications are available from http://www.pcisig.com.

a) *PCI specification, revision 3.0*.
b) *PCI Express specification, revision 2.1*.
c) *PCI Express® Card Electromechanical Specification, Revision 2.0.* April 11, 2007. Commonly known as the "PCIe CEM" spec.

SFF specifications are available from ftp://ftp.seagate.com/sff

a) *SFF-8680* Serial Attachment 12 Gb/s 2x Unshielded Connector, Rev 1.6 July 11, 2012. Commonly known as the "12G SAS connector" spec.
b) SFF-8201 Specification for Form Factor of 2.5" Disk Drives**,** Rev 2.4, May 30, 2005.
c) SFF-8301 Specification for Form Factor of 3.5" Disk Drives**,** Rev 1.6, March 16, 2010
d) *SFF-8639 Specification for Multifunction 12 Gb/s 6X Unshielded Connector, Rev* 1.4, October 9, 2012.

4.6.2 Formal Bibliography

*PC*I SIG. *PCIe Specifications*. Retrieved from PCI SIG specifcations: http://www.pciesig.com

SFF. *SFF Specifcations*. Retrieved from SFF Web Site: http://ftp.seagate.com/sff

4.7 Specification Conventions

4.7.1 Definitions

4.7.1.1 PCI Express® (PCIe)

The PCI Express IO bus standard, please see the 4.6.1for a list of the most relevant PCIe documents (PCI SIG).

4.7.1.2 PCI Express® Generation 2 (PCIe Gen2)

In this context PCIe Gen2 is used to refer to a link speed of 5Gbps using 8b/10b encoding.

4.7.1.3 PCI Express® Generation 3 (PCIe Gen3)

In this context PCIe Gen3 is used to refer to a link speed 8Gbps using a 128/130 encoding with scrambling.

4.7.1.4 PCI Express® x2 (PCIe x2)

X2 means using 2 PCIe lanes for communication. This is 2 differential pairs in each direction. Total signals is 2 lanes times 2 (differential) times 2 (Transmit and receive) = 8 signals.

4.7.1.5 SFF standards

SFF Committee is an ad hoc group that defined the 2.5 inch drive and related specification. Documents created by the SFF Committee are submitted to bodies such as EIA (Electronic Industries Association) or an ASC (Accredited Standards Committee).

4.7.1.6 SSD

Solid State Drive.