Serial ATA International Organization

Version 1.0.1RC1
10 October 2007

Serial ATA Interoperability Program Revision 1.2 Pre-Test MOI

TABLE OF CONTENTS

MODIFICATION RECORD

2007 Oct 10 (r1.2, v1.0.1RC1) UPDATE for r1.2, v1.0.1 INTEROP PROGRAM

Andy Baldman (UNH-IOL): Appendix B: Added 2-ALIGN pattern (preferred), in addition to existing 4-ALIGN pattern
Appendix B: Added references to external ASCII-binary pattern .txt files (to be included with MOI.)
Appendix C: Reformatted table to fit on one page.
General: Cleaned up page/paragraph formatting across entire document.

(EARLIER DRAFTS FOR 1.0, 1.1, and 1.2 SATA-IO INTEROP PROGRAM REVS)

2007 Apr 06 (v0.90) DRAFT RELEASE FOR 1.2 INTEROP PROGRAM

Andy Baldman (UNH-IOL): Appendix B: Updated framed COMP pattern to make ALIGNs always occur in bursts of 4. Also, added additional D10.2 Dwords following the frame (i.e. in the inter-packet gap) to change overall pattern length from 84480 to 92160 bits, so ensure that proper ALIGN sequence spacing of 256 Dwords is always maintained when pattern is repeated end-to-end.
Appendix C: Added 'Informative' to title of appendix.

2006 Nov 13 (v0.99) DRAFT RELEASE

David Woolf (UNH-IOL): Title page edits.

2006 Oct 19 (v0.98) DRAFT RELEASE

David Woolf (UNH-IOL): Fixed another error in the framed COMP pattern.

2006 Sep 28 (v0.97) DRAFT RELEASE

David Woolf (UNH-IOL): Fixed error in the framed COMP pattern.

2006 Sep 21 (v0.96) DRAFT RELEASE

David Woolf (UNH-IOL): Added note that Stimulus tool in Ready State Operation 01 should have Power Management diabled.
Clarified use of the framed COMP pattern.
Changed name of document from "BIST Activate MOI" to "Pre-Test MOI".

2006 Sep 20 (v0.95) DRAFT RELEASE

David Woolf (UNH-IOL): Fixed framed COMP pattern in Appendix B. Added Worst Case Port Identification and Ready State Operation tests. Added SSC checking to BIST-L and BIST-T tests.

2006 Sep 14 (v0.94) DRAFT RELEASE

Andy Baldman (UNH-IOL): Fixed framed COMP pattern in Appendix B.

2006 Sep 05 (v0.93) DRAFT RELEASE

David Woolf (UNH-IOL): Editorial Changes

2006 Aug 31 (v0.92) DRAFT RELEASE

David Woolf (UNH-IOL): Edited Figure A-2

2006 Aug 31 (v0.91) DRAFT RELEASE

David Woolf (UNH-IOL): Editorial Changes

2006 Aug 28 (v0.90) INITIAL DRAFT RELEASE

David Woolf (UNH-IOL): Initial Release

ACKNOWLEDGMENTS

The Serial ATA Logo Group would like to acknowledge the efforts of the following individuals in the development of this document:

David Woolf	University of New Hampshire InterOperability Lab (UNH-IOL)	djwoolf@iol.unh.edu
Andy Baldman	University of New Hampshire InterOperability Lab (UNH-IOL)	aab@iol.unh.edu
Jeff Wolford	Hewlett-Packard	jeff.wolford@hp.com

INTRODUCTION

The tests contained in this document are organized in order to simplify the identification of information related to a test, and to facilitate in the actual testing process. Tests are separated into groups, primarily in order to reduce setup time in the lab environment, however the different groups typically also tend to focus on specific aspects of product functionality.

The test definitions themselves are intended to provide a high-level description of the motivation, resources, procedures, and methodologies specific to each test. Formally, each test description contains the following sections:

Purpose

The purpose is a brief statement outlining what the test attempts to achieve. The test is written at the functional level.

References

This section specifies all reference material *external* to the test suite, including the specific subclauses references for the test in question, and any other references that might be helpful in understanding the test methodology and/or test results. External sources are always referenced by a bracketed number (e.g., [1]) when mentioned in the test description. Any other references in the test description that are not indicated in this manner refer to elements within the test suite document itself (e.g., "Appendix 6.A", or "Table 6.1.1-1")

Resource Requirements

The requirements section specifies the test hardware and/or software needed to perform the test. This is generally expressed in terms of minimum requirements, however in some cases specific equipment manufacturer/model information may be provided.

Last Modification

This specifies the date of the last modification to this test.

Discussion

The discussion covers the assumptions made in the design or implementation of the test, as well as known limitations. Other items specific to the test are covered here as well.

Test Setup

The setup section describes the initial configuration of the test environment. Small changes in the configuration should not be included here, and are generally covered in the test procedure section (next).

Procedure

The procedure section of the test description contains the systematic instructions for carrying out the test. It provides a cookbook approach to testing, and may be interspersed with observable results.

Observable Results

This section lists the specific observables that can be examined by the tester in order to verify that the PUT is operating properly. When multiple values for an observable are possible, this section provides a short discussion on how to interpret them. The determination of a pass or fail outcome for a particular test is generally based on the successful (or unsuccessful) detection of a specific observable.

Possible Problems

This section contains a description of known issues with the test procedure, which may affect test results in certain situations. It may also refer the reader to test suite appendices and/or other external sources that may provide more detail regarding these issues.

GROUP 1: READY STATE OPERATION

Overview:

This group of tests verifies the functionality of the product under test when it is in the HR_Ready or DR_Ready state, depending on if the product is a host or a device. These tests are primarily for information gathering, to facilitate testing of SATA Spec requirements. These tests do not provide comprehensive coverage of all requirements covered by the SATA v2.5 spec.

Test Ready State Operation 01 - Ready State Operation

Purpose: To determine the behavior of the product under test in the HR/DR_Ready state.

References:

[1] SATA Standard 2.5

Resource Requirements:

See Appendix A for more.

- Stimulus Tool: Any device or system capable of :
  i. Generating SATA OOB and Speed Negotiation and bringing the PUT to the Ready State (HR_Ready or DR_Ready) at all speeds supported by the PUT.
  ii. Generating SATA NRZ signaling with and without SSC .
  iii. Disabling SATA Power Management
- Monitoring Tool: Any device or system capable of receiving and decoding valid non-framed, non-primitive SATA NRZ signaling, and recovering clock frequency.

Last Modification: September 4, 2007

Discussion:

Before performing electrical measurements on a product, it is often useful to understand the behavior of the product. This test procedure is designed to procure information about the behavior of a product when in the HR/DR_Ready state, or the normal operation state of a SATA product after OOB and Speed Negotiation have completed. In this test information about the products data transmissions, support for SSC, DC offset, and supported bit rates is gathered. This information will facilitate later electrical testing.

Test Setup: See Appendix A

Test Procedure:

- PUT is completely booted has completed OOB and completed all necessary actions to maintain activity on the Port attached to the Stimulus Tool. The Stimulus tool should be transmitting SATA NRZ Signaling with SSC enabled. Record the information listed in the Observable Results below.
- Disable SSC on the transmitter of the Stimulus tool. Repeat the entire procedure for each bit rate supported by the PUT.

Observable Results:

- Record the bit rate of the PUT.
- Record whether the PUT transmitter has a DC offset. If the median amplitude value of the transmitted signal from the PUT is non-zero, then a DC offset is present.
- Record if the PUT is transmitting data with SSC enabled. This can determined by a clock frequency measurement taken over 30.3 microseconds (1 SSC period of 33 kHz).
- Record what the PUT transmits when it is in the HR/DR Ready state. The device may be transmitting ALIGN or SYNC primitives, or random Idle data characters.

Possible Problems: None.

GROUP 2: BIST-T REQUIREMENTS

Overview:

This group of tests verifies BIST-T functionality, for the purposes of performing SATA-IO Interoperability Testing. These tests are limited to functionality which impacts the Interoperability tests only, and do not provide comprehensive coverage of all BIST requirements covered by the SATA v2.5 spec.

Test BIST-T 01 - BIST-TAS Operation

Purpose: To verify that the Product Under Test (PUT) properly responds to a received BIST-TAS FIS.

References:

[1] SATA Standard 2.5, 10.3.9 – BIST Activate

Resource Requirements:

See Appendix A for more.

- Stimulus Tool: Any device or system capable of :
  i. Generating SATA OOB and Speed Negotiation and bringing the PUT to a state where it can receive a BIST Activate FIS.
  ii. Generating a BIST Activate FIS.
- Monitoring Tool: Any device or system capable of receiving and decoding valid non-framed, non-primitive SATA NRZ signaling.

Last Modification: September 4, 2007

Discussion:

Reference [1] specifies how a SATA Host or Device can be configured in a Built In Self Test (BIST) Mode by receiving a BIST Activate FIS. Depending on the contents of the BIST Activate FIS a product can be put into different BIST operation modes. If bits 23:21 of the first dword of the FIS is set to 1 and bits 20:16 are set to 0, the BIST Activate FIS should enable BIST-TAS operation in the PUT. BIST-TAS is defined as Far End Transmit mode, with ALIGN insertion and scrambling bypassed. In this mode the product under test will transmit the pattern contained in the second and third dwords of the BIST Activate FIS without inserting ALIGN primitives and without scrambling the pattern before transmitting it. This test is to be performed with each of the following patterns in the BIST Activate FIS: HFTP, LFTP, MFTP, LBP.

Test Setup: See Appendix A

Test Procedure:

- PUT is completely booted has completed OOB and completed all necessary actions to maintain activity on the Port attached to the Stimulus Tool.
- The Stimulus Tool should transmit a BIST-TAS with one of the patterns indicated in the discussion.
- After the BIST-TAS FIS is sent the Stimulus Tool should transmit SATA Dwords, SYNC, or ALIGN. The Stimulus Tool should not send any COMINIT/COMRESET, COMWAKE signals or Electrical Idle.
- Record if the PUT is transmitting data with SSC enabled. This can determined by a clock frequency measurement taken over 30.3 microseconds (1 SSC period of 33 kHz).
- Repeat the entire procedure for each of the 4 patterns and each speed supported by the PUT.

Observable Results:

- Using the Monitoring Tool, verify that the PUT sources the correct pattern which was in the BIST-TAS FIS, that the pattern is not scrambled, and that the PUT does not source any ALIGN primitives.

Possible Problems: None.

Test BIST-T 02 - BIST-TAS Disconnect (Informative)

Purpose: To verify that the Product Under Test (PUT) can maintain the BIST-TAS state following a disconnect event. Note that this test is informative, as support for disconnect is not required by the SATA v2.5 spec.

References:

[1] SATA Standard 2.5, 10.3.9 – BIST Activate

Resource Requirements: See Appendix A for more.

- Stimulus Tool: Any device or system capable of :
  i. Generating SATA OOB and Speed Negotiation and bringing the PUT to a state where it can receive a BIST Activate FIS.
  ii. Generating a BIST Activate FIS.
- Monitoring Tool: Any device or system capable of receiving and decoding valid non-framed, non-primitive SATA NRZ signaling.

Last Modification: September 4, 2007

Discussion:

Reference [1] specifies how a SATA Host or Device can be configured in a Built In Self Test (BIST) Mode by receiving a BIST Activate FIS. When testing SATA products it is often necessary to enable a BIST mode with one tool (SATA Device Emulator or SATA Protocol Generator) and perform a measurement on the transmitted signal with another tool (e.g., Digital Oscilloscope). Test Setup and execution is less complicated when the PUT remains in BIST operation when disconnected. Some PUTs will leave BIST operation when disconnected and source OOB or other signals. When a PUT behaves this way the tests that depend on the BIST modes need to be performed in such a way that the PUT does not exit BIST operation. These test methods are more complicated and time-consuming than the methods used for PUTs that remain in BIST operation when disconnected. One method for testing a PUT that does not remain in BIST operation when disconnected is to continuously provide the PUT with transitioning signal and sourcing that signal from 2 sources using a power combiner/divider. The transmitter of the Stimulus Tool must continue to transmit valid SATA Signaling including SYNC and ALIGN primitives. The Stimulus Tool must not transmit OOB signals or turn off its signal when the receiver of the Stimulus Tool is disconnected. The aim of this test is to determine if such methods are necessary when testing a product.

Test Setup: See Appendix A

Test Procedure:

- Perform the procedure from test BIST-TAS 01 get PUT into BIST-TAS mode sourcing any one of the patterns mentioned in the previous test.
- If allowed by the physical setup, disconnect and reconnect the cables from only the transmitter of the PUT and verify that PUT still is sending the pattern from the BIST Activate FIS sourced from the Stimulus Tool.
- Disconnect the cable from the transmitter and the receiver of the PUT then reconnect the cable. Verify that the PUT continues to send the pattern from the BIST Activate FIS sourced from the Stimulus Tool and does not source COMINIT/COMRESET, Electric Idle or any other primitives or dwords not included in the pattern from the Stimulus Tool.
- Using the Stimulus Tool send COMINIT/RESET, verify that the PUT responds with COMINIT/RESET.
- Repeat the test procedure at each supported speed of the PUT.

Observable Results:

- Using the Monitoring Tool, verify that the PUT sources the correct pattern which was in the BIST-TAS FIS, that the pattern is not scrambled, and that the PUT does not source any ALIGN primitives after each of the disconnects from transmitter only and from transmitter and receiver respectively. Finally verify that the PUT responds to COMINIT/COMRESET by resetting and responding with COMINIT/COMRESET.

Possible Problems: None.

GROUP 3: BIST-L REQUIREMENTS

Overview:

This group of tests verifies BIST-L functionality, for the purposes of performing SATA-IO Interoperability Testing. These tests are limited to functionality which impacts the Interoperability tests only, and do not provide comprehensive coverage of all BIST requirements covered by the SATA v2.5 spec.

Test BIST-L 01 - BIST-L Operation

Purpose: To verify that the Product Under Test (PUT) properly responds to a received BIST-L FIS.

References:

[1] SATA Standard 2.5, 10.3.9 – BIST Activate

Resource Requirements: See Appendix A for more.

- Stimulus Tool: Any device or system capable of :
  i. Generating SATA OOB and Speed Negotiation and bringing the PUT to a state where it can receive a BIST Activate FIS.
  ii. Generating a BIST Activate FIS.
  iii. Generating a looping frame pattern continuously.
- Monitoring Tool: Any device capable of:
  i. receiving and decoding valid SATA frames and primitives.
  ii. Allowing ALIGN primitives to be added/dropped by the PUT from the data stream as allowed by Reference [1], and not detecting the added/dropped ALIGNs as an error.

Last Modification: September 4, 2007

Discussion:

Reference [1] specifies how a SATA Host or Device can be configured in a Built In Self Test (BIST) Mode by receiving a BIST Activate FIS. Depending on the contents of the BIST Activate FIS a product can be put into different BIST operation modes. If bit 20 of the first dword of the FIS is set to 1 and bits 23:21 and 19:16 are set to 0, the BIST Activate FIS should enable BIST-L operation in the product under test. BIST-L is defined as Far End Retimed Loopback mode. In this mode the product under test receives and retimes data and retransmits the retimed data.

Reference [1] specifies that the PUT shall return all received data unaltered and disregard protocol processing of primitives. All data except ALIGN primitives and OOB signals are retransmitted without interpretation. The BIST-L operation mode is designed for use in implementing a receiver stress test on products and proper implementation of BIST-L in a product is essential to performing such testing. Minimally, the signal source should transmit a framed COMP pattern to verify BIST-L operation. To exhaustively test all possible SATA primitives and 10b codes, a suggested test pattern for verifying BIST-L operation is included in Appendix C, which includes all 10b patterns and all SATA primitives.

Test Setup: See Appendix A

Procedure:

- PUT is completely booted. This means that the product has been powered on, is in the HR/DR_Ready state and had completed any other necessary actions to maintain activity on the Port being tested. The Stimulus tool should be transmitting SATA NRZ Signaling with SSC enabled.
- The Stimulus Tool should transmit a BIST-L FIS followed by a framed pattern. The Stimulus Tool will transmit the framed pattern continuously. Verify Observable Results below.
- Record if the PUT is transmitting data with SSC enabled. This can determined by a clock frequency measurement taken over 30.3 microseconds (1 SSC period of 33 kHz).
- Disable SSC on the transmitter of the Stimulus tool. Repeat the entire procedure for each bit rate supported by the PUT.

Observable Results:

- Using the Monitoring Station, verify that the PUT forwards framed pattern exactly as it is transmitted from the Stimulus Tool and does not insert or substitute primitives or dwords other than ALIGN.
- Using the Monitoring Station, verify that the PUT does not remove primitives or dwords other than ALIGN

Possible Problems: Some products, hosts in particular, may need to reach a certain stage in the boot process before they will respond to a BIST Activate FIS. In such cases BIST may be enabled by using a Device Emulator, SCT Disk Drive, or a vendor unique tool.

Test BIST-L 02 - BIST-L Disconnect (Informative)

Purpose: To verify that the Product Under Test (PUT) can maintain the BIST-L state following a disconnect event. Note that this test is informative, as support for disconnect is not required by the SATA v2.5 spec.

References:

[1] SATA Standard 2.5, 10.3.9 – BIST Activate

Resource Requirements: See Appendix A for more.

- Stimulus Tool: Any device or system capable of :
  i. Generating SATA OOB and Speed Negotiation and bringing the PUT to a state where it can receive a BIST Activate FIS.
  ii. Generating a BIST Activate FIS.
  iii. Generating a looping frame pattern continuously.
- Monitoring Tool: Any device capable of:
  i. receiving and decoding valid SATA frames and primitives.
  ii. Allowing ALIGN primitives to be added/dropped by the PUT from the data stream as allowed by Reference [1], and not detecting the added/dropped ALIGNs as an error.

Last Modification: September 4, 2007

Discussion:

Reference [1] specifies how a SATA Host or Device can be configured in a BIST Mode by receiving a BIST Activate FIS. When testing SATA products it is often necessary to enable a BIST mode with one tool (SATA Device Emulator; SATA Protocol Generator; Bit Error Rate Tester; Pattern Generator; or Arbitrary Waveform Generator) and perform a measurement on the transmitted signal with another tool (Oscilloscope; Bit error Rate Tester; or TDR). Test Setup and execution is less complicated when the PUT remains in BIST operation when disconnected. Some PUTs will leave BIST operation when disconnected and source OOB or other signals. When a PUT behaves this way the tests that depend on the BIST modes need to be performed in such a way that the PUT does not exit BIST operation. These test methods are more complicated and time-consuming than the methods used for PUTs that remain in BIST operation when disconnected. One method for testing a PUT that does not remain in BIST operation when disconnected is to continuously provide the PUT with transitioning signal and sourcing that signal from 2 sources using a power combiner/divider. The transmitter of the Stimulus Tool must continue to transmit valid SATA Signaling including SYNC and ALIGN primitives. The Stimulus Tool must not transmit OOB signals or turn off its signal when the receiver of the Stimulus Tool is disconnected. The aim of this test is to determine if such methods are necessary when testing a product.

Test Setup: See Appendix A

Procedure:

- Perform the procedure from test BIST-L 01 to get the PUT into BIST-L mode.
- If allowed by the physical setup, disconnect and reconnect the cables from only the transmitter of the PUT and verify that PUT still is sending the pattern being sourced from the Stimulus Tool.
- Disconnect the cable from the transmitter and the receiver of the PUT then reconnect the cable. Verify that the PUT continues to send the pattern being sourced by the Stimulus Tool and does not source COMINIT/RESET, Electric Idle or any other primitives or dwords not included in the pattern from the Stimulus Tool.
- Using the Stimulus Tool send COMINIT/RESET, verify that the PUT responds with COMINIT/RESET.
- Repeat the entire test procedure at each supported speed of the PUT.

Observable Results:

- Using the Monitoring Tool, verify that after each disconnect and reconnect step, the PUT does not source COMINIT/RESET, Electric Idle or any other primitives or dwords not included in the pattern from the Stimulus Tool, but only continues to source the pattern being transmitted by the Stimulus Tool once the receiver of the PUT is reconnected to the Stimulus Tool.
- Using the Monitoring Tool, verify that the PUT does not insert, substitute, or remove primitives or dwords other than ALIGN.
- Using the Monitoring Tool, verify that the PUT responds to the COMINIT/COMRESET sourced by the Stimulus Tool with COMINIT/COMRESET.

Possible Problems: None.

GROUP 4: WORST CASE PORT IDENTIFICATION

Overview:

To save time when performing electrical measurements on a multi-port product, it is useful to determine the worst port, and perform the electrical measurements on that port, in the assumption that the other ports will perform better. This test describes how to determine the worst port.

Test Worst Case Port Identification 01 - Total Jitter Measurement

Purpose: To determine the electrically worst port on a multi-port device

References:

[1] SATA Standard, 7.2.1, Table 22 – Transmitted Signal Requirements
[2] SATA Interoperability Program Unified Test Document

Resource Requirements:

See Appendix A for more.

- Paired Product: A SATA Host, Device, or Test Tool capable of connecting to the PUT across the High Impedance Splitter tap and keeping the PUT in the HR/DR_Ready state at all speeds supported by the PUT.
- Monitoring Tool: Any device or system capable of performing a TJ measurement on SATA NRZ signaling.
- High Impedance Splitter Tap: A tap, which will present a proper termination for the Monitoring Tool as well the PUT.

Last Modification: September 4, 2007

Discussion:

To save time when performing electrical measurements on a multi-port product, it is useful to determine the worst port, and perform the electrical measurements on that port, in the assumption that the other ports will perform better. When determining the worst-case port, it is only necessary to determine the worst port within the PUT, relative to the other ports. A convenient metric for this is Total Jitter at each port. Since the measurement is relative, ideal test fixtures or specific test modes are not needed. The easiest way to perform this test is by connecting the PUT to a paired device through a high impedance splitter tap to get it into the HR/DR_Ready state, and then measuring the TJ of the PUT transmitter through the high impedance splitter tap.

Test Setup: See Appendix A

Test Procedure:

- PUT and Paired Product are completely booted and the PUT is in the HR/DR_Ready state while connected through the High Impedance Splitter Tap. The PUT and Paired Product should be connected at the highest supported speed of the PUT.
- Perform a TJ measurement on the connected port.
- Repeat the above procedure for each port on the PUT.

Observable Results:

- Record the value of the TJ for each port on the device. The port with the highest value should be recorded as the worst port. Further electrical measurements should be performed on this port.

Possible Problems: None.

APPENDICES

Overview:

Test suite appendices are intended to provide additional low-level technical detail pertinent to specific tests contained in this test suite. These appendices often cover topics that are outside of the scope of the standard, and are specific to the methodologies used for performing the measurements in this test suite. Appendix topics may also include discussion regarding a specific interpretation of the standard (for the purposes of this test suite), for cases where a particular specification may appear unclear or otherwise open to multiple interpretations.

Test suite appendices are considered informative supplements, and pertain solely to the test definitions and procedures contained in this test suite.

Appendix A – Resource Requirements and Test Setup

Purpose: To define the hardware/software requirements and basic test setup used for all tests in this test suite.

References:
None.

Last Modification: September 20, 2006

Discussion:

A.1 - Introduction

It is necessary to monitor the transmitter of the product under test throughout the test procedures defined in this document.

A.2 - Equipment

The list below summarizes possible implementations of the Monitoring Tool described in this appendix:

- Real Time Digital Oscilloscope
- Sampling Digital Oscilloscope
- Bit Error Rate Tester
- SATA Protocol Analyzer
- Logic Analyzer

The list below summarizes possible implementations of the Stimulus Tool described in this appendix:

- SATA Host System with special software
- SATA Protocol Generator
- SATA Device Emulator
- SCT Disk Drive
- Bit Error Rate Tester
- Pattern Generator
- Arbitrary Waveform Generator
- Any combination of the above

A.3- Diagram of Test Setup

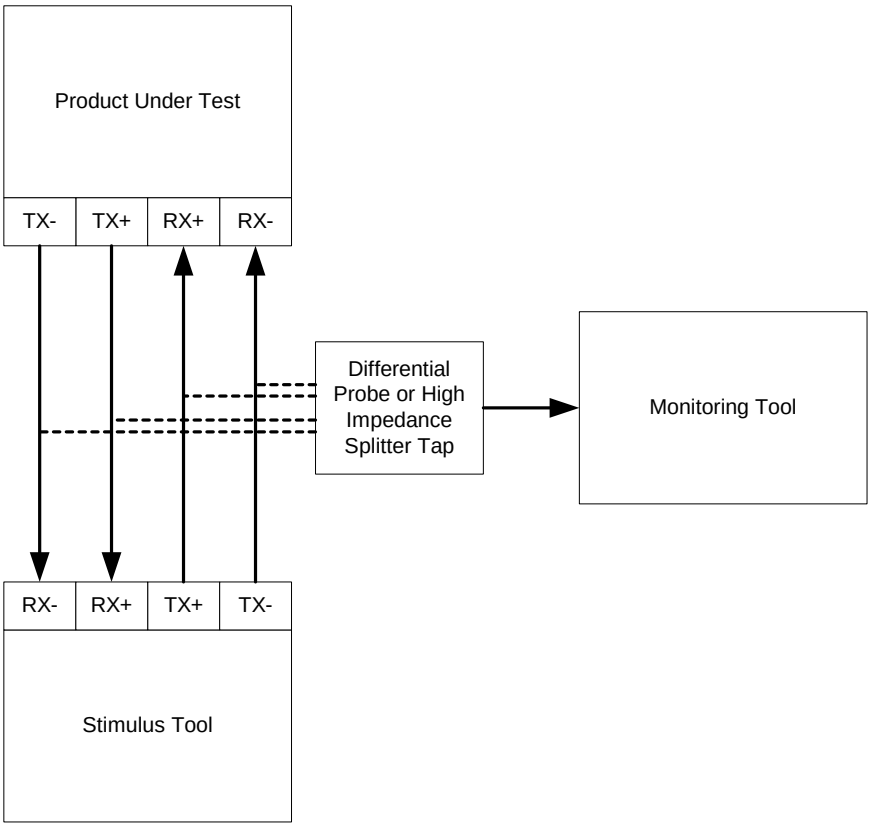

Figure A-1: Test Setup using a single device as a Stimulus Tool. Note that if worst-case port identification is being performed with the above setup, it is advisable to use a High Impedance Splitter Tap instead of a differential probe

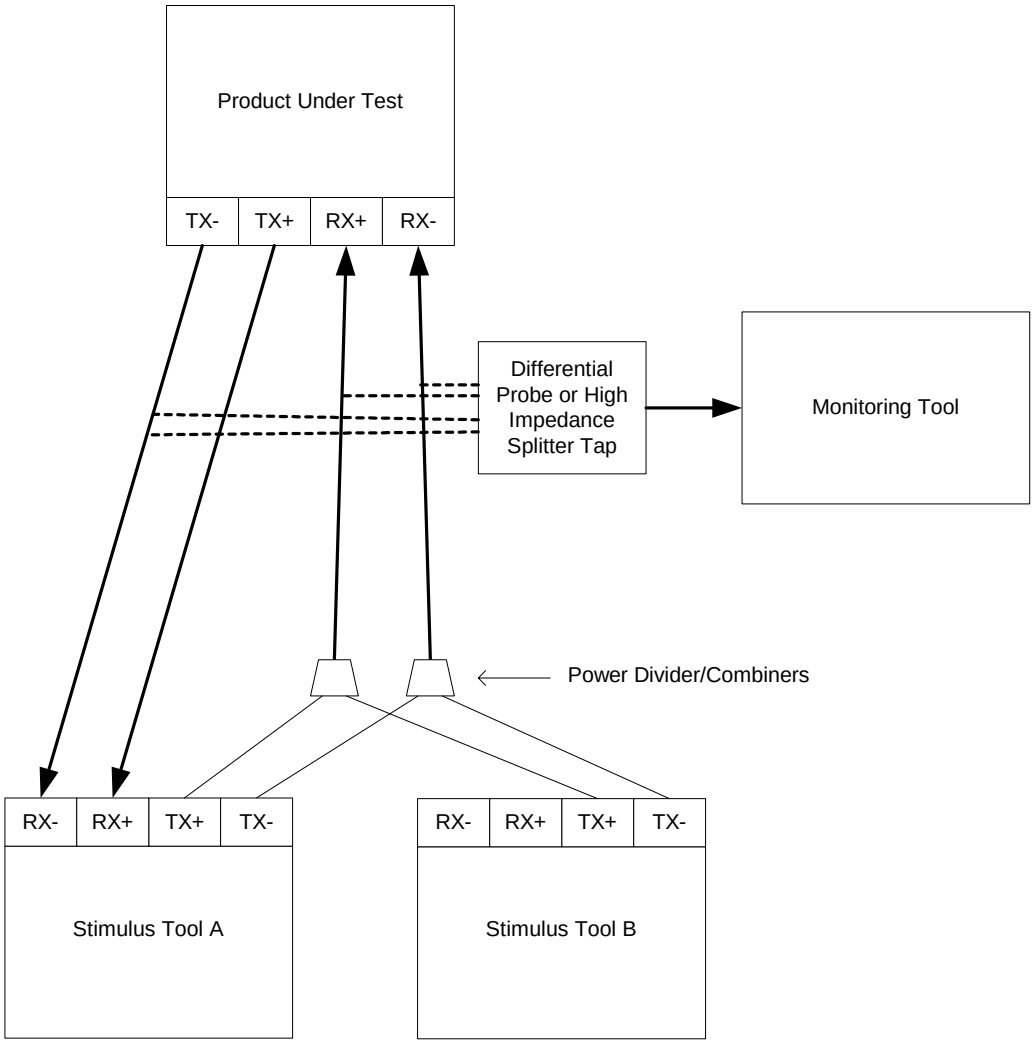

Figure A-2: Test Setup using two Stimulus Tools with different capabilities in combination by using a Power Combiner between the transmitters of the Stimulus Tool and the receiver of the Product Under Test to ensure that the Product Under Test always is receiving signaling. It may be necessary to boost transmitter amplitude from the Stimulus Tool in order to compensate for the Power Divider, to ensure that the Stimulus Tool and the PUT are able to maintain a connection.

Appendix B – Framed COMP Pattern

Purpose: To define a framed version of the COMP pattern that may be used to verify BIST-L operation.

References:
SATA Standard 2.5, 7.2.4.3.6 Composite Pattern

Last Modification: October 10, 2007

Discussion:
This appendix actually defines two versions of the framed version of the COMP pattern. Both patterns have been specifically created to satisfy all of the following design criteria:

- Properly framed version of the COMP pattern. (SOF/HEADER/CRC/EOF)
- Contains leading X_RDY and trailing WTRM/SYNC/CONT primitives to maintain framing protocol consistency.
- Maintains running disparity. (Pattern begins and ends with the same running disparity, so that when it is transmitted continuously, the Monitoring Tool does not detect the leading SOF as a Running Disparity error.)
- Maintains desired ALIGN count and spacing. (First *n* dwords are ALIGN out of every group of 256 dwords, where N is two/four for the first/second version of the pattern, respectively).
- Maintains ALIGN spacing upon wrapping. (Requires total pattern length to be an even multiple of 40*256=10240 bits. 92160=9*10240.)
- Overall pattern length is even multiple of 128/256/512 bits, for broad compatibility with known pattern generators.

Note that these patterns have been specifically designed for SATA-IO test purposes. ***Any deletion/insertion of data, or other modification to the exact bit sequence will render the pattern invalid for the purposes of Revision 1.2 SATA-IO RSG testing.***

The two defined versions of the pattern differ only in terms of the number of ALIGNs occurring in each ALIGN sequence. The first version contains two ALIGNs in each ALIGN burst. The second version contains four ALIGNs per burst. Both patterns are the same number of bits in length (92160), and contain identical frame contents. The IPG length of the 4-ALIGN pattern is slightly shorter, to account for the additional ALIGN primitives, and still keep the overall bit length consistent between the two pattern versions.

Note that the 2-ALIGN version is considered the recommended version, but the 4-ALIGN version may also be used for backwards compatibility.

Also note that the raw bit patterns are provided in external .txt files, which should accompany this document (and may also be downloaded from the SATA-IO website.)

B.1 – 2-ALIGN Framed COMP Pattern *(Recommended pattern)*

(NOTE: A full ASCII-binary version of this pattern is provided in the external text file: *Framed_COMP_20070907_2ALIGNs_oldLBP_92160_bits_BITS_ONLY.txt*)

```
   1: +K28.5- BC 1100000101  -D10.2- 4A 0101010101  -D10.2- 4A 0101010101  -D27.3+ 7B 1101100011  ALIGN
                                    (Repeat previous Dword until)
   3: +D10.2+ 4A 0101010101  +D10.2+ 4A 0101010101  +D10.2+ 4A 0101010101  +D10.2+ 4A 0101010101
                                    (Repeat previous Dword until)
  10: +K28.3- 7C 1100001100  -D21.5- B5 1010101010  -D23.2+ 57 1110100101  +D23.2- 57 0001010101  X_RDY
  11: -K28.3+ 7C 0011110011  +D21.5+ B5 1010101010  +D23.2- 57 0001010101  -D23.2+ 57 1110100101  X_RDY
  12: +K28.3- 7C 1100001100  -D21.5- B5 1010101010  -D23.2+ 57 1110100101  +D23.2- 57 0001010101  X_RDY
  13: -K28.3+ 7C 0011110011  +D21.5+ B5 1010101010  +D23.2- 57 0001010101  -D23.2+ 57 1110100101  X_RDY
  14: +K28.3- 7C 1100001100  -D21.5- B5 1010101010  -D23.2+ 57 1110100101  +D23.2- 57 0001010101  X_RDY
  15: -K28.3+ 7C 0011110011  +D21.5+ B5 1010101010  +D23.1- 37 0001011001  -D23.1+ 37 1110101001  SOF
  16: +D11.6+ CB 1101000110  +D22.3+ 76 0110100011  +D18.6+ D2 0100110110  + D2.6- C2 0100100110
  17: -D31.3+ 7F 1010110011  +D31.3- 7F 0101001100  -D31.3+ 7F 1010110011  +D31.3- 7F 0101001100
                                    (Repeat previous Dword until)
 257: -K28.5+ BC 0011111010  +D10.2+ 4A 0101010101  +D10.2+ 4A 0101010101  +D27.3- 7B 0010011100  ALIGN
                                    (Repeat previous Dword until)
 259: -D31.3+ 7F 1010110011  +D31.3- 7F 0101001100  -D31.3+ 7F 1010110011  +D31.3- 7F 0101001100
                                    (Repeat previous Dword until)
 275: -D21.5- B5 1010101010  -D21.5- B5 1010101010  -D21.5- B5 1010101010  -D21.5- B5 1010101010
                                    (Repeat previous Dword until)
 339: -D24.3+ 78 1100110011  +D24.3- 78 0011001100  -D24.3+ 78 1100110011  +D24.3- 78 0011001100
                                    (Repeat previous Dword until)
 403: -D10.2- 4A 0101010101  -D10.2- 4A 0101010101  -D10.2- 4A 0101010101  -D10.2- 4A 0101010101
                                    (Repeat previous Dword until)
 467: -D25.6- D9 1001100110  - D6.1- 26 0110011001  -D25.6- D9 1001100110  - D6.1- 26 0110011001
                                    (Repeat previous Dword until)
 513: -K28.5+ BC 0011111010  +D10.2+ 4A 0101010101  +D10.2+ 4A 0101010101  +D27.3- 7B 0010011100  ALIGN
                                    (Repeat previous Dword until)
 515: -D25.6- D9 1001100110  - D6.1- 26 0110011001  -D25.6- D9 1001100110  - D6.1- 26 0110011001
                                    (Repeat previous Dword until)
 533: -D17.7+ F1 1000110111  +D30.7+ FE 1000011110  + D7.1+ 27 0001111001  +D14.7- EE 0111001000
 534: -D30.7- FE 0111100001  - D7.6- C7 1110000110  -D30.3+ 7E 0111100011  +D30.3- 7E 1000011100
 535: -D30.3+ 7E 0111100011  +D30.3- 7E 1000011100  -D30.3+ 7E 0111100011  +D30.3- 7E 1000011100
                                    (Repeat previous Dword until)
 769: -K28.5+ BC 0011111010  +D10.2+ 4A 0101010101  +D10.2+ 4A 0101010101  +D27.3- 7B 0010011100  ALIGN
                                    (Repeat previous Dword until)
 771: -D30.3+ 7E 0111100011  +D30.3- 7E 1000011100  -D30.3+ 7E 0111100011  +D30.3- 7E 1000011100
                                    (Repeat previous Dword until)
1025: -K28.5+ BC 0011111010  +D10.2+ 4A 0101010101  +D10.2+ 4A 0101010101  +D27.3- 7B 0010011100  ALIGN
                                    (Repeat previous Dword until)
1027: -D30.3+ 7E 0111100011  +D30.3- 7E 1000011100  -D30.3+ 7E 0111100011  +D30.3- 7E 1000011100
                                    (Repeat previous Dword until)
1048: - D3.7+ E3 1100011110  +D28.7- FC 0011100001  - D3.7+ E3 1100011110  +D28.7- FC 0011100001
1049: -D12.0+ 0C 0011011011  +D11.4- 8B 1101000010  -D12.0+ 0C 0011011011  +D11.4- 8B 1101000010  -LBPorig
                                    (Repeat previous Dword until)
1281: -K28.5+ BC 0011111010  +D10.2+ 4A 0101010101  +D10.2+ 4A 0101010101  +D27.3- 7B 0010011100  ALIGN
                                    (Repeat previous Dword until)
1283: -D12.0+ 0C 0011011011  +D11.4- 8B 1101000010  -D12.0+ 0C 0011011011  +D11.4- 8B 1101000010  -LBPorig
                                    (Repeat previous Dword until)
1307: -D20.2- 54 0010110101  -D20.2- 54 0010110101  -D20.2- 54 0010110101  -D20.2- 54 0010110101
                                    (Repeat previous Dword until)
1537: -K28.5+ BC 0011111010  +D10.2+ 4A 0101010101  +D10.2+ 4A 0101010101  +D27.3- 7B 0010011100  ALIGN
                                    (Repeat previous Dword until)
1539: -D20.2- 54 0010110101  -D20.2- 54 0010110101  -D20.2- 54 0010110101  -D20.2- 54 0010110101
                                    (Repeat previous Dword until)
1564: -D20.2- 54 0010110101  -D20.7+ F4 0010110111  +D11.5+ AB 1101001010  +D11.5+ AB 1101001010
1565: +D11.5+ AB 1101001010  +D11.5+ AB 1101001010  +D11.5+ AB 1101001010  +D11.5+ AB 1101001010
                                    (Repeat previous Dword until)
1793: +K28.5- BC 1100000101  -D10.2- 4A 0101010101  -D10.2- 4A 0101010101  -D27.3+ 7B 1101100011  ALIGN
                                    (Repeat previous Dword until)
1795: +D11.5+ AB 1101001010  +D11.5+ AB 1101001010  +D11.5+ AB 1101001010  +D11.5+ AB 1101001010
                                    (Repeat previous Dword until)
1822: +D11.5+ AB 1101001010  +D11.7- EB 1101001000  -D20.2- 54 0010110101  -D20.2- 54 0010110101
1823: -D21.5- B5 1010101010  -D21.5- B5 1010101010  -D21.5- B5 1010101010  -D21.5- B5 1010101010
                                    (Repeat previous Dword until)
1887: -D24.3+ 78 1100110011  +D24.3- 78 0011001100  -D24.3+ 78 1100110011  +D24.3- 78 0011001100
                                    (Repeat previous Dword until)
1951: -D10.2- 4A 0101010101  -D10.2- 4A 0101010101  -D10.2- 4A 0101010101  -D10.2- 4A 0101010101
                                    (Repeat previous Dword until)
2015: -D25.6- D9 1001100110  - D6.1- 26 0110011001  -D25.6- D9 1001100110  - D6.1- 26 0110011001
                                    (Repeat previous Dword until)
2049: -K28.5+ BC 0011111010  +D10.2+ 4A 0101010101  +D10.2+ 4A 0101010101  +D27.3- 7B 0010011100  ALIGN
                                    (Repeat previous Dword until)
```

```
2051: -D25.6- D9 1001100110  - D6.1- 26 0110011001  -D25.6- D9 1001100110  - D6.1- 26 0110011001
                                    (Repeat previous Dword until)
2081: -D22.4+ 96 0110101101  +D16.0+ 10 1001001011  + D9.3+ 69 1001010011  +D28.4- 9C 0011100010
2082: -K28.3+ 7C 0011110011  +D21.5+ B5 1010101010  +D21.6+ D5 1010100110  +D21.6+ D5 1010100110  EOF
2083: +K28.3- 7C 1100001100  -D21.5- B5 1010101010  -D24.2+ 58 1100110101  +D24.2- 58 0011000101  WTRM
2084: -K28.3+ 7C 0011110011  +D21.5+ B5 1010101010  +D24.2- 58 0011000101  -D24.2+ 58 1100110101  WTRM
2085: +K28.3- 7C 1100001100  -D21.5- B5 1010101010  -D24.2+ 58 1100110101  +D24.2- 58 0011000101  WTRM
2086: -K28.3+ 7C 0011110011  +D21.5+ B5 1010101010  +D24.2- 58 0011000101  -D24.2+ 58 1100110101  WTRM
2087: +K28.3- 7C 1100001100  -D21.4+ 95 1010101101  +D21.5+ B5 1010101010  +D21.5+ B5 1010101010  SYNC
                                    (Repeat previous Dword until)
2089: +K28.3- 7C 1100001100  -D10.5- AA 0101011010  -D25.4+ 99 1001101101  +D25.4- 99 1001100010  CONT
2090: -K28.3+ 7C 0011110011  +D10.5+ AA 0101011010  +D25.4- 99 1001100010  -D25.4+ 99 1001101101  CONT
2091: +D10.2+ 4A 0101010101  +D10.2+ 4A 0101010101  +D10.2+ 4A 0101010101  +D10.2+ 4A 0101010101
                                    (Repeat previous Dword until)
2304: +D10.2+ 4A 0101010101  +D10.2+ 4A 0101010101  +D10.2+ 4A 0101010101  +D10.2+ 4A 0101010101
```

B.2 – 4-ALIGN Framed COMP Pattern *(Recommended for backward compatibility purposes only, if DUT cannot support 2-ALIGN pattern)*

(NOTE: A full ASCII-binary version of this pattern is provided in the external text file: *Framed_COMP_20070406_4ALIGNs_oldLBP_92160_bits_BITS_ONLY.txt*)

```
   1: +K28.5- BC 1100000101  -D10.2- 4A 0101010101  -D10.2- 4A 0101010101  -D27.3+ 7B 1101100011  ALIGN
                                    (Repeat previous Dword until)
   5: +D10.2+ 4A 0101010101  +D10.2+ 4A 0101010101  +D10.2+ 4A 0101010101  +D10.2+ 4A 0101010101
                                    (Repeat previous Dword until)
  10: +K28.3- 7C 1100001100  -D21.5- B5 1010101010  -D23.2+ 57 1110100101  +D23.2- 57 0001010101  X_RDY
  11: -K28.3+ 7C 0011110011  +D21.5+ B5 1010101010  +D23.2- 57 0001010101  -D23.2+ 57 1110100101  X_RDY
  12: +K28.3- 7C 1100001100  -D21.5- B5 1010101010  -D23.2+ 57 1110100101  +D23.2- 57 0001010101  X_RDY
  13: -K28.3+ 7C 0011110011  +D21.5+ B5 1010101010  +D23.2- 57 0001010101  -D23.2+ 57 1110100101  X_RDY
  14: +K28.3- 7C 1100001100  -D21.5- B5 1010101010  -D23.2+ 57 1110100101  +D23.2- 57 0001010101  X_RDY
  15: -K28.3+ 7C 0011110011  +D21.5+ B5 1010101010  +D23.1- 37 0001011001  -D23.1+ 37 1110101001  SOF
  16: +D11.6+ CB 1101000110  +D22.3+ 76 0110100011  +D18.6+ D2 0100110110  + D2.6- C2 0100100110
  17: -D31.3+ 7F 1010110011  +D31.3- 7F 0101001100  -D31.3+ 7F 1010110011  +D31.3- 7F 0101001100
                                    (Repeat previous Dword until)
 257: -K28.5+ BC 0011111010  +D10.2+ 4A 0101010101  +D10.2+ 4A 0101010101  +D27.3- 7B 0010011100  ALIGN
                                    (Repeat previous Dword until)
 261: -D31.3+ 7F 1010110011  +D31.3- 7F 0101001100  -D31.3+ 7F 1010110011  +D31.3- 7F 0101001100
                                    (Repeat previous Dword until)
 277: -D21.5- B5 1010101010  -D21.5- B5 1010101010  -D21.5- B5 1010101010  -D21.5- B5 1010101010
                                    (Repeat previous Dword until)
 341: -D24.3+ 78 1100110011  +D24.3- 78 0011001100  -D24.3+ 78 1100110011  +D24.3- 78 0011001100
                                    (Repeat previous Dword until)
 405: -D10.2- 4A 0101010101  -D10.2- 4A 0101010101  -D10.2- 4A 0101010101  -D10.2- 4A 0101010101
                                    (Repeat previous Dword until)
 469: -D25.6- D9 1001100110  - D6.1- 26 0110011001  -D25.6- D9 1001100110  - D6.1- 26 0110011001
                                    (Repeat previous Dword until)
 513: -K28.5+ BC 0011111010  +D10.2+ 4A 0101010101  +D10.2+ 4A 0101010101  +D27.3- 7B 0010011100  ALIGN
                                    (Repeat previous Dword until)
 517: -D25.6- D9 1001100110  - D6.1- 26 0110011001  -D25.6- D9 1001100110  - D6.1- 26 0110011001
                                    (Repeat previous Dword until)
 537: -D17.7+ F1 1000110111  +D30.7+ FE 1000011110  + D7.1+ 27 0001111001  +D14.7- EE 0111001000
 538: -D30.7- FE 0111100001  - D7.6- C7 1110000110  -D30.3+ 7E 0111100011  +D30.3- 7E 1000011100
 539: -D30.3+ 7E 0111100011  +D30.3- 7E 1000011100  -D30.3+ 7E 0111100011  +D30.3- 7E 1000011100
                                    (Repeat previous Dword until)
 769: -K28.5+ BC 0011111010  +D10.2+ 4A 0101010101  +D10.2+ 4A 0101010101  +D27.3- 7B 0010011100  ALIGN
                                    (Repeat previous Dword until)
 773: -D30.3+ 7E 0111100011  +D30.3- 7E 1000011100  -D30.3+ 7E 0111100011  +D30.3- 7E 1000011100
                                    (Repeat previous Dword until)
1025: -K28.5+ BC 0011111010  +D10.2+ 4A 0101010101  +D10.2+ 4A 0101010101  +D27.3- 7B 0010011100  ALIGN
                                    (Repeat previous Dword until)
1029: -D30.3+ 7E 0111100011  +D30.3- 7E 1000011100  -D30.3+ 7E 0111100011  +D30.3- 7E 1000011100
                                    (Repeat previous Dword until)
1056: - D3.7+ E3 1100011110  +D28.7- FC 0011100001  - D3.7+ E3 1100011110  +D28.7- FC 0011100001
1057: -D12.0+ 0C 0011011011  +D11.4- 8B 1101000010  -D12.0+ 0C 0011011011  +D11.4- 8B 1101000010  -LBPorig
                                    (Repeat previous Dword until)
1281: -K28.5+ BC 0011111010  +D10.2+ 4A 0101010101  +D10.2+ 4A 0101010101  +D27.3- 7B 0010011100  ALIGN
                                    (Repeat previous Dword until)
1285: -D12.0+ 0C 0011011011  +D11.4- 8B 1101000010  -D12.0+ 0C 0011011011  +D11.4- 8B 1101000010  -LBPorig
                                    (Repeat previous Dword until)
1317: -D20.2- 54 0010110101  -D20.2- 54 0010110101  -D20.2- 54 0010110101  -D20.2- 54 0010110101
                                    (Repeat previous Dword until)
1537: -K28.5+ BC 0011111010  +D10.2+ 4A 0101010101  +D10.2+ 4A 0101010101  +D27.3- 7B 0010011100  ALIGN
                                    (Repeat previous Dword until)
1541: -D20.2- 54 0010110101  -D20.2- 54 0010110101  -D20.2- 54 0010110101  -D20.2- 54 0010110101
                                    (Repeat previous Dword until)
1576: -D20.2- 54 0010110101  -D20.7+ F4 0010110111  +D11.5+ AB 1101001010  +D11.5+ AB 1101001010
1577: +D11.5+ AB 1101001010  +D11.5+ AB 1101001010  +D11.5+ AB 1101001010  +D11.5+ AB 1101001010
                                    (Repeat previous Dword until)
1793: +K28.5- BC 1100000101  -D10.2- 4A 0101010101  -D10.2- 4A 0101010101  -D27.3+ 7B 1101100011  ALIGN
                                    (Repeat previous Dword until)
1797: +D11.5+ AB 1101001010  +D11.5+ AB 1101001010  +D11.5+ AB 1101001010  +D11.5+ AB 1101001010
                                    (Repeat previous Dword until)
1836: +D11.5+ AB 1101001010  +D11.7- EB 1101001000  -D20.2- 54 0010110101  -D20.2- 54 0010110101
1837: -D21.5- B5 1010101010  -D21.5- B5 1010101010  -D21.5- B5 1010101010  -D21.5- B5 1010101010
                                    (Repeat previous Dword until)
1901: -D24.3+ 78 1100110011  +D24.3- 78 0011001100  -D24.3+ 78 1100110011  +D24.3- 78 0011001100
                                    (Repeat previous Dword until)
1965: -D10.2- 4A 0101010101  -D10.2- 4A 0101010101  -D10.2- 4A 0101010101  -D10.2- 4A 0101010101
                                    (Repeat previous Dword until)
2029: -D25.6- D9 1001100110  - D6.1- 26 0110011001  -D25.6- D9 1001100110  - D6.1- 26 0110011001
                                    (Repeat previous Dword until)
2049: -K28.5+ BC 0011111010  +D10.2+ 4A 0101010101  +D10.2+ 4A 0101010101  +D27.3- 7B 0010011100  ALIGN
                                    (Repeat previous Dword until)
```

```
2053: -D25.6- D9 1001100110  - D6.1- 26 0110011001  -D25.6- D9 1001100110  - D6.1- 26 0110011001
                                    (Repeat previous Dword until)
2097: -D22.4+ 96 0110101101  +D16.0+ 10 1001001011  + D9.3+ 69 1001010011  +D28.4- 9C 0011100010
2098: -K28.3+ 7C 0011110011  +D21.5+ B5 1010101010  +D21.6+ D5 1010100110  +D21.6+ D5 1010100110  EOF
2099: +K28.3- 7C 1100001100  -D21.5- B5 1010101010  -D24.2+ 58 1100110101  +D24.2- 58 0011000101  WTRM
2100: -K28.3+ 7C 0011110011  +D21.5+ B5 1010101010  +D24.2- 58 0011000101  -D24.2+ 58 1100110101  WTRM
2101: +K28.3- 7C 1100001100  -D21.5- B5 1010101010  -D24.2+ 58 1100110101  +D24.2- 58 0011000101  WTRM
2102: -K28.3+ 7C 0011110011  +D21.5+ B5 1010101010  +D24.2- 58 0011000101  -D24.2+ 58 1100110101  WTRM
2103: +K28.3- 7C 1100001100  -D21.4+ 95 1010101101  +D21.5+ B5 1010101010  +D21.5+ B5 1010101010  SYNC
                                    (Repeat previous Dword until)
2105: +K28.3- 7C 1100001100  -D10.5- AA 0101011010  -D25.4+ 99 1001101101  +D25.4- 99 1001100010  CONT
2106: -K28.3+ 7C 0011110011  +D10.5+ AA 0101011010  +D25.4- 99 1001100010  -D25.4+ 99 1001101101  CONT
2107: +D10.2+ 4A 0101010101  +D10.2+ 4A 0101010101  +D10.2+ 4A 0101010101  +D10.2+ 4A 0101010101
                                    (Repeat previous Dword until)
2304: +D10.2+ 4A 0101010101  +D10.2+ 4A 0101010101  +D10.2+ 4A 0101010101  +D10.2+ 4A 0101010101
```

Appendix C – Full BIST-L Verification Pattern (Informative)

Purpose: To define a Data Pattern containing all valid SATA primitives and 10B codewords, which can be used to fully exercise BIST-L operation.

References: None.

Last Modification: April 6, 2007

Discussion:

C.1 - Data Pattern

The following data pattern contains all defined SATA Primitives and a frame that contains all valid 10b characters. This is the pattern that should appear 'on the wire' when transmitted by the Stimulus Tool continuously to verify proper BIST-L operation in the Product Under Test:

	Primitive/ Dword		Primitive/ Dword		Primitive/ Dword		Primitive/ Dword
1	ALIGN	45	X_RDY	89	43454647	133	9A9CA0A1
2	ALIGN	46	SOF	90	494A4B4C	134	A2A4A8AF
3	ALIGN	47	03000102	91	4D4E5152	135	B0B7B8BB
4	CONT	48	04080F10	92	53545556	136	BDBEBFC0
5	CONT	49	17181B1D	93	595A5C63	137	C1C2C4C8
6	CONT	50	1E1F2325	94	65666769	138	CFD0D7D8
7	HOLD	51	2627292A	95	6A6B6C6D	139	DBDDDEDF
8	HOLD	52	2B2C2D2E	96	6E717273	140	E3E5E6E7
9	HOLD	53	31323334	97	74757679	141	E9EAEBEC
10	HOLDA	54	3536393A	98	7A7C8081	142	EDEEF1F2
11	HOLDA	55	3C434546	99	8284888F	143	F3F4F5F6
12	HOLDA	56	47494A4B	100	9097989B	144	F9FAFC05
13	PMACK	57	4C4D4E51	101	9D9E9FA3	145	0607090A
14	PMACK	58	52535455	102	A5A6A7A9	146	0B0C0D0E
15	PMACK	59	56595A5C	103	AAABACAD	147	11121314
16	PMNAK	60	63656667	104	AEB1B2B3	148	1516191A
17	PMNAK	61	696A6B6C	105	B4B5B6B9	149	1C202122
18	PMNAK	62	6D6E7172	106	BABCC3C5	150	24282F30
19	PMREQ_P	63	73747576	107	C6C7C9CA	151	37383B3D
20	PMREQ_P	64	797A7C80	108	CBCCCDCE	152	3E3F4041
21	PMREQ_P	65	81828488	109	D1D2D3D4	153	4244484F
22	PMREQ_S	66	8F909798	110	D5D6D9DA	154	5057585B
23	PMREQ_S	67	9B9D9E9F	111	DCE0E1E2	155	5D5E5F60
24	PMREQ_S	68	A3A5A6A7	112	E4E8EFF0	156	61626468
25	R_ERR	69	A9AAABAC	113	F7F8FBFD	157	6F707778
26	R_ERR	70	ADAEB1B2	114	FEFF0506	158	7B7D7E7F
27	R_ERR	71	B3B4B5B6	115	07090A0B	159	83858687
28	R_IP	72	B9BABCC3	116	0C0D0E11	160	898A8B8C
29	R_IP	73	C5C6C7C9	117	12131415	161	8D8E9192
30	R_IP	74	CACBCCCD	118	16191A1C	162	93949596
31	R_OK	75	CED1D2D3	119	20212224	163	999A9CA0
32	R_OK	76	D4D5D6D9	120	282F3037	164	A1A2A4A8
33	R_OK	77	DADCE0E1	121	383B3D3E	165	AFB0B7B8
34	R_RDY	78	E2E4E8EF	122	3F404142	166	BBBDBEBF
35	R_RDY	79	F0F7F8FB	123	44484F50	167	C0C1C2C4
36	R_RDY	80	FDFEFF03	124	57585B5D	168	C8CFD0D7
37	SYNC	81	00102040	125	5E5F6061	169	D8DBDDDE
38	SYNC	82	080F1017	126	6264686F	170	DFE3E5E6
39	SYNC	83	181B1D1E	127	7077787B	171	E7E9EAEB
40	WTRM	84	1F232526	128	7D7E7F83	172	ECEDEEF1
41	WTRM	85	27292A2B	129	85868789	173	F2F3F4F5
42	WTRM	86	2C2D2E31	130	8A8B8C8D	174	F6F9FAFC
43	X_RDY	87	32333435	131	8E919293	175	EOF
44	X_RDY	88	36393A3C	132	94959699		