Serial ATA International Organization

Version: 1.0 Revision 1.6
18 February 2020

Serial ATA Interoperability Program Revision 1.6 Keysight Technologies, Inc. Method of Implementation (MOI) Document for SATA PHY, TSG & OOB Measurements (Real-time Oscilloscope (DSO/DSA models) Measurements)

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MODIFICATION RECORD

January 16, 2006 (Version 1.0 template) INITIAL RELEASE, TO LOGO TF MOI GROUP
Andy Baldman: Initial Release

February 7, 2006 (Version 0.8) INITIAL RELEASE, TO LOGO TF MOI GROUP
Bryan Kantack: Initial Release

February 20, 2006 (Version 0.9)
Bryan Kantack: Updates made to reflect IW Event #1 Unified Test Document changes

March 17, 2006 (Version 0.91)
Bryan Kantack: General formatting, Update SATA templates to Rev 2.0 for all measurements

April 3, 2006 (Version 0.92)
Bryan Kantack: Removal of TX/RX test sections, incorporation of first-pass reviewer feedback

May 7, 2006 (Version 0.93)
Bryan Kantack: Update SATA templates to Rev 2.1 for all measurements; OOB timing updates for OOB-01 through OOB-07

May 25, 2006 (Version 0.94)
Bryan Kantack: General formatting and updates to align with Unified Test Document Rev 1.0RC2i (May 11, 2006); added Unified Test Document section references to each measurement

June 8, 2006 (Version 0.95)
Bryan Kantack: Update to OOB-01 OOB Detection Threshold procedure (removed two unnecessary tests)

June 9, 2006 (Version 0.95RC) REVIEW RELEASE, TO LOGO TF MOI GROUP
Bryan Kantack: Release to LOGO TF MOI Group for final review and vote

June 19, 2006 (Version 0.96RC)
Bryan Kantack: Update TSG-01, TSG-02, TSG-09, TSG-10, PHY-02, PHY-04 text per reviewer feedback; changed COMAX part number H303000204 to H303000204 to correctly reference new product revision; edited typographical error in OOB-04 through OOB-07 test descriptions; incorporation of final reviewer feedback

June 21, 2006 (Version 1.0RC) REVIEW RELEASE, TO LOGO TF MOI GROUP
Bryan Kantack: Release to LOGO TF MOI Group for final review and vote

June 22, 2006 (Version 1.0RC2) REVIEW RELEASE, TO LOGO TF MOI GROUP
Bryan Kantack: Release to LOGO TF MOI Group for final review and vote; updated PHY-04 and TSG-02 text per committee feedback

September 26, 2006 (Version 1.0RC3) REVIEW RELEASE, TO LOGO TF MOI GROUP
Fei Xie: Release to LOGO TF MOI Group for review and vote on changes to include products testing and PHY-02, PHY-04 updates.

September 28, 2006 (Version 0.99a)
Fei Xie: Updated to include host as well as device testing.

October 11, 2006 (Version 0.99b)
Fei Xie: Define nominal values for PHY02 and PHY04.

November 15, 2006 (Version 0.99c)
Fei Xie: Added Accuracy Table in Appendix

December 13th, 2006 (Version 0.99d)

Fei Xie: PHY02 Procedure detail

January 9th, 2007 (Version 0.99e)

Fei Xie: PHY02 Procedure detail with screenshot.

January 31st, 2007 (Version 0.99f)

Fei Xie: OOB 01, 06, 07 update to new method. Jitter algorithm update to new method. Added return loss Appendix

October 31st, 2007 (Version 0.9 Revision 1.3) new nomenclature adopted by LOGO

Bryan Kantack: Updated PHY-02 and PHY-04 measurement detail per ECN 016 changes. Updated OOB-02, OOB-03, OOB-04, OOB-05 measurement detail per ECN 017 changes. Updated TSG-07 & TSG-08 to be INFORMATIVE per ECN 006. Updated TSG-09, TSG-10, TSG-11 & TSG-12 per ECN 008. Updated TSG-09, TSG-10, TSG-11 & TSG-12 clock recovery settings per the approved Jitter Transfer Function definition. Added Appendix for the Calibration and Verification of Jitter Measurement Devices.

December 14th, 2007 (Version 0.9 Revision 1.3) new nomenclature adopted by LOGO

Bryan Kantack: Accepted all red-line edits and comments per LOGO committee walk-through. Incorporated new JTF calibration documentation to include calibration of both 1.5Gpbs and 3.0Gbps clock recovery settings used for TSG-09 through TSG-12, in accordance with the procedure used to calibrate the Agilent DSA91204A JMD for Interoperability Workshop #4, November 12-16, 2007.

February 26th, 2008 (Version 0.91 Revision 1.3) new nomenclature adopted by LOGO

Bryan Kantack: Replaced typographical references to Serial ATA Revision 2.5 with updated references to Serial ATA Revision 2.6. Updated OOB-01 test procedure to include automated amplitude calibration procedure for 81134A stimulus.

June 5th, 2008 (Version 0.93 Revision 1.3)

Bryan Kantack: Updated references to Unified Test Document 1.3 resource tables and sections. Added clarification to calibration of OOB Threshold measurements in OOB-01. Added graphics to Appendix E, Calibration of Jitter Measurement Devices, to clarify process steps.

June 12th, 2008 (Version 1.0RC Revision 1.3)

Bryan Kantack: Document red-line changes reviewed and accepted. Voted into approval by SATA-IO LOGO committee and rolled version to 1.0RC.

July 25th, 2008 (Version 1.0 Revision 1.3)

Bryan Kantack: Passed 30-day member review. Released as Version 1.0 Revision 1.3

March 25th, 2009 (Version 0.8 Revision 1.4)

Bryan Kantack: Updated per Unified Test Document Revision 1.4 and SATA Revision 3.0 Specificatio n changes; added TSG-013 through TSG-016; updated Appendix E for 6Gb/s JTF calibration procedure

May 28th, 2009 (Version 1.0RC Revision 1.4)

Bryan Kantack: Moved to 1.0RC status per unanimous LOGO committee vote in acceptance of all proposed revisions and successful results correlation through IW#7 dry-run testing.

August 19th, 2009 (Version 1.0RC2 Revision 1.4)

Min-Jie Chong: Updated per Unified Test Document Revision 1.4 V1.00RC2. Moved TSG-05 and TSG-06 to obsolete status.

August 27th, 2009 (Version 1.0 Revision 1.4)

Min-Jie Chong: Passed 30-day member review. Released as Version 1.0 Revision 1.4

September 16th, 2010 (Version 1.08 Revision 1.4)

Min-Jie Chong:

Added Agilent DSAX93204A oscilloscope to the equipment list.

Updated document to include total jitter at 1E-6 and 1E-12 measurements per ECN-39 as normative and the previously defined jitter test requirements as informative only.

Added Wilder Technologies SATA Gen3 Receptacle Adapter SATA-TPA-R and ICT-Lanto SATA Receptacle Gen 3 TF-1R31 Test Fixtures.

Added section outlining SerialTek BusMod BusGen BIST Generator as an alternate BIST mode and pattern generation tool.

Updated clock recovery settings for the oscilloscope JTF requirements.

Cleaned up language and document formatting.

October 27th, 2010 (Version 1.10RC Revision 1.4)

Min-Jie Chong:
Updated Agilent DSAX93204A, DSAX92804A, DSAX92504A, DSAX92004A and DSAX91604A oscilloscope models to the equipment list.
Updated OOB-06 Comwake sequence gap values in accordance to the change in UTD 1.4 version 1.01.

January 20th, 2011 (Version 1.10 Revision 1.4)

Min-Jie Chong:
Passed 30-day member review. Released as Version 1.10 Revision 1.4

May 3rd, 2013 (Version 0.80 Revision 1.5)

Min-Jie Chong:
Added N4903B J-BERT as BIST initiator tool
Move TSG-02 and TSG-03 to informative
Move TSG-16 to obsolete (ECN 56)
Modified TSG-04 to include Gen 1u, 2u, 3u and 3i requirements (ECN 56/66)
Modified TSG-13 to remove CIC when testing UHost (Gen 3u)
Modified TSG-15 to measure direct eye with 5MUI instead of 1E-12 extrapolation, as well as asymmetrical spec limit for Host (200mV) and Device (240mV) (ECN50)
Modified TSG-15 to remove CIC when testing UHost (Gen 3u)
Modified OOB tests to include N4903B J-BERT
Modified OOB-06/07 to increase gap width for Host
Modified calibration procedure in Appendix B
Updated the Agilent scope software revision from 1.02 to 1.65

January 6th, 2016 (Version 0.9RC Revision 1.5)

Matthew Woerner:
Added TSG-17
Changed Agilent to Keysight
Updated the Keysight Oscilloscope software revision from 1.65 to 1.82

February 5th, 2020 (Version 0.9RC Revision 1.6)

Vincent Yew:
Updated reference of SATA Revision 3.2/UTD Revision 1.5 to Serial ATA Revision 3.4/UTD Revision 1.6
Updated the title row of limits table in TSG-17 (it was empty in previous document)
Changed Agilent to Keysight in PHY-01
Corrected some typo on Keysight name in OOB-01, OOB-02 and OOB-06

February 6th, 2020 (Version 0.91RC Revision 1.6)

John Calvin:
Updated TSG-17 to include the alternate procedure outlined in SATA 3.4 section 7.6.33.4 Peak-Mode Device TX Emphasis

February 7th, 2020 (Version 0.92RC Revision 1.6)

Vincent Yew:
Added D9030SATC (current solution nomenclature) to N5411B (legacy solution)
John Calvin, Kayla Seliner (Novus labs):
Introduced a OOB-06[a],-06[b] manual workaround for HUT's that support ASR timing greater than that permitted by current D9030SATC test automation systems.

ACKNOWLEDGMENTS

Keysight Technologies, Inc. would like to acknowledge the efforts of the following individuals in the development of this document.

SATA MOI Template Creation	Andrew Baldman	University of New Hampshire Interoperability Lab
	David Woolf	University of New Hampshire Interoperability Lab
Keysight PHY Test MOI Creation	Bryan Kantack	Agilent Technologies, Inc.
	Fei Xie	Agilent Technologies, Inc.
	Min-Jie Chong	Agilent Technologies, Inc.
	Matthew Woerner	Keysight Technologies, Inc.
	Vincent Yew	Keysight Technologies, Inc.
	John Calvin	Keysight Technologies, Inc.

INTRODUCTION

The tests contained in this document are organized in order to simplify the identification of information related to a test, and to facilitate in the actual testing process. Tests are separated into groups, primarily in order to reduce setup time in the lab environment, however the different groups typically also tend to focus on specific aspects of products functionality.

The test definitions themselves are intended to provide a high-level description of the motivation, resources, procedures, and methodologies specific to each test. Formally, each test description contains the following sections:

Purpose

The purpose is a brief statement outlining what the test attempts to achieve. The test is written at the functional level.

References

This section specifies all reference material *external* to the test suite, including the specific subclauses references for the test in question, and any other references that might be helpful in understanding the test methodology and/or test results. External sources are always referenced by a bracketed number (e.g., [1]) when mentioned in the test description. Any other references in the test description that are not indicated in this manner refer to elements within the test suite document itself (e.g., “Appendix 6.A”, or “Table 6.1.1-1”)

Resource Requirements

The requirements section specifies the test hardware and/or software needed to perform the test. This is generally expressed in terms of minimum requirements, however in some cases specific equipment manufacturer/model information may be provided.

Last Modification

This specifies the date of the last modification to this test.

Discussion

The discussion covers the assumptions made in the design or implementation of the test, as well as known limitations. Other items specific to the test are covered here as well.

Test Setup

The setup section describes the initial configuration of the test environment. Small changes in the configuration should not be included here, and are generally covered in the test procedure section (next).

Procedure

The procedure section of the test description contains the systematic instructions for carrying out the test. It provides a cookbook approach to testing, and may be interspersed with observable results.

Observable Results

This section lists the specific observables that can be examined by the tester in order to verify that the product is operating properly. When multiple values for an observable are possible, this section provides a short discussion on how to interpret them. The determination of a pass or fail outcome for a particular test is generally based on the successful (or unsuccessful) detection of a specific observable.

Possible Problems

This section contains a description of known issues with the test procedure, which may affect test results in certain situations. It may also refer the reader to test suite appendices and/or other external sources that may provide more detail regarding these issues.

REFERENCES

This method of implementation document references the following texts:

- Serial ATA Revision 3.4 (SATA Revision 3.4)
- Serial ATA Interoperability Program Unified Test Document Revision 1.6
- Serial ATA Interoperability Program Policy Document Revision 1.4
- Serial ATA Interoperability Program Pre-Test MOI Revision 1.4 (Pre-Test MOI) PHY

GENERAL REQUIREMENTS

Overview:

This group of tests verifies the Phy General Requirements, as defined in Section 2.13 of the Serial ATA Interoperability Unified Test Document, Revision 1.6 (which references Serial ATA Revision 3.4).

Test PHY-01 - Unit Interval

Purpose: To verify that the Unit Interval of the Product Under Test (PUT) TX signaling is within the conformance limits.

References:

[1] Serial ATA Revision 3.0, 7.2.1, Table 29 – General Specifications
[2] Ibid, 7.2.2.1.3 – Unit Interval
[3] Ibid, 7.4.14 – SSC Profile
[4] SATA Interoperability Program Unified Test Document, 2.13.1 – Unit Interval
[5] Pre-Test MOI

Resource Requirements:

- Keysight DSAX93204A, DSAX92804A, DSAX92504A, DSAX92004A and DSAX91604A (32GHz, 28GHz, 25GHz, 20GHz and 16GHz bandwidth, 80GS/s per channel) or Keysight DSA91204A (12GHz bandwidth, 40GS/s per channel)
- Keysight N5411B (legacy solution) AND D9030SATC (current solution nomenclature) SATA 6 Gb/s Compliance Test Software
- Wilder Technologies SATA Gen3 Receptacle Adapter SATA-TPA-R or ICT-Lanto SATA Receptacle Gen 3 TF-1R31 or Crescent Heart Software TF-SATA-NE/ZP or TF-eSATA-NE/ZP test adapter or equivalent
- Keysight N4903B J-BERT (with Option 002), Gen3i capable products PC running ULink, SerialTek BusMod BusGen BIST Generator or any other mechanism that makes the products produce the required patterns is acceptable.

See appendix A for details.

Last Template Modification: May 3, 2013 (Version 1.65)

Discussion:

Reference [1] specifies the general PHY conformance limits for SATA products. This specification includes conformance limits for the mean Unit Interval (UI). Reference [2] provides the definition of this term for the purposes of SATA testing. Reference [3] defines the measurement requirements for this test.

In this test, the mean UI value is measured based on the average of at least 100,000 observed UI's, measured at the transmitter output.

The mean UI is measured from a Unit Interval measurement trend, after a low-pass filter with 1.98MHz -3dB bandwidth, and applies to signaling with SSC enabled and/or disabled. This value includes the frequency long-term stability deviation and the Spread Spectrum Clock FM frequency deviation.

Test Setup:

1. (For Hosts only) select the worst case port as described in reference [5]. All further connections to the products would be to the worst case port.

2. The N5411B (legacy solution) AND D9030SATC (current solution nomenclature) automated test software will prompt you to make the products produce HFTP. Once prompted, follow the procedures in the respective sections in reference [5] to either activate BIST-TAS HFTP pattern or BIST-L if BIST-L is supported by the products.

3. Plug the test fixture into the products. The test fixture is connected to channels 1 and 3 of the scope by two 36" SMA cables (Rosenberger or equivalent). OBSERVE the signal on the scope. If it is HFTP, press OK in the N5411B (legacy solution) AND D9030SATC (current solution nomenclature) prompt. If not,

the products did not properly handle BIST Activate FIS; a non-standard way to make it produce the desired pattern will be required.

Test Procedure:

This parameter is covered by Keysight Technologies, Inc. N5411B (legacy solution) AND D9030SATC (current solution nomenclature) automated SATA compliance software, revision 1.65 or later. Either "PASS" or "FAIL" is shown for the unit interval test in the report generated at the completion of the testing. Both Min and Max tests must pass to pass the unit interval test.

Observable Results:

- PHY-01a - Mean Unit Interval measured between 666.4333ps (min) to 670.2333ps (max) (for products running at 1.5Gb/s)
- PHY-01b - Mean Unit Interval measured between 333.2167ps (min) to 335.1167ps (max) (for products running at 3Gb/s)
- PHY-01c – Mean Unit Interval measured between 166.6083ps (min) to 167.5583ps (max) (for products running at 6Gb/s)
- The values above shall be based on at least 100,000 UIs (covers at least one SSC profile)

Possible Problems:

Some products may not support disconnect during the process of enabling BIST and testing. For these products, refer to the Disconnect sections of reference [5] for setup requirement.

Test PHY-02 – Frequency Long Term Accuracy

Purpose: To verify that the long term frequency stability of the Products Under Test's (PUT's) transmitter is within the conformance limit.

References:

[1] Serial ATA Revision 3.0, 7.2.1, Table 29 – General Specifications
[2] Ibid, 7.2.2.1.4 – TX Frequency Long Term Stability
[3] Ibid, 7.4.7 – Long Term Frequency Accuracy
[4] SATA Interoperability Program Unified Test Document, 2.12.2 – Frequency Long-Term Stability
[5] Pre-Test MOI

Resource Requirements:

Same requirements as for PHY-01

Last Template Modification: May 3, 2013 (Version 1.65)

Discussion:

Reference [1] specifies the general PHY conformance limits for SATA products. Reference [2] provides the definition of this term for the purposes of SATA testing. Reference [3] defines the measurement requirements for this test. This test is not performed for products employing SSC since SSC modulation deviation and frequency long-term accuracy cannot be separated in measurement. For products employing SSC, PHY-04 will measure the total UI deviation.

This test is only run once at the maximum interface rate of the products (1.5Gb/s, 3.0Gb/s or 6.0Gb/s)

Test Setup:

Same setup as for PHY-01.

Test Procedure:

This parameter is covered by Keysight Technologies, Inc. N5411B (legacy solution) AND D9030SATC (current solution nomenclature) automated SATA compliance software, revision 1.65 or later. The Mean frequency is measured and reported for non SSC productss. Either "PASS" or "FAIL" is shown for the SSC frequency test in the report generated at the completion of the testing.

Mean Test: (Measured Mean – Nominal)/Nominal)* 1E6 < +/-350 ppm for pass

where Nominal is defined as 1.5E9 for Gen 1 products, 3E9 for Gen 2 products and 6E9 for Gen 3 products.

Observable Results:

The value of the Mean Test at the maximum interface rate is considered for the non-SSC enabled products. The Frequency Long Term Accuracy value shall be between +/-350ppm. products.

Possible Problems:

Some products may not support disconnect during the process of enabling BIST and testing. For these products, refer to the Disconnect sections of reference [5] for setup requirement.

Test PHY-03 - Spread-Spectrum Modulation Frequency

Purpose: To verify that the Spread Spectrum Modulation Frequency of the Products Under Test's (PUT) transmitter is within the conformance limits.

References:

[1] Serial ATA Revision 3.0, 7.2.1, Table 29 – General Specifications
[2] Ibid, 7.2.2.1.5 – Spread-Spectrum Modulation Frequency
[3] Ibid, 7.4.14 – SSC Profile
[4] SATA Interoperability Program Unified Test Document, 2.13.3 – Spread-Spectrum Modulation Frequency
[5] Pre-Test MOI

Resource Requirements:

Same requirements as for PHY-01

Last Template Modification: May 3, 2013 (Version 1.65)

Discussion:

Reference [1] specifies the general PHY conformance limits for SATA products. This specification includes conformance limits for the Spread-Spectrum Modulation Frequency. Reference [2] provides the definition of this term for the purposes of SATA testing. Reference [3] defines the measurement requirements for this test.

In this test, the Spread-Spectrum Modulation Frequency, f_{SSC}, is measured, based on at least 10 complete SSC cycles.

This test is only run once at the maximum interface rate of the product (1.5Gb/s, 3.0Gb/s or 6.0Gb/s)

Test Setup:

Same setup as for PHY-01.

Test Procedure:

This parameter is covered by Keysight Technologies, Inc. N5411B (legacy solution) AND D9030SATC (current solution nomenclature) automated SATA compliance software, revision 1.65 or later. The Mean frequency is measured at the 50% threshold of the Unit Interval trend and reported. The Mean is cumulative over all acquisitions and the final Mean SSC modulation frequency is reported as the final value. Either "PASS" or "FAIL" is shown for the SSC frequency test in the report generated at the completion of the testing.

Observable Results:

The Spread-Spectrum Modulation Frequency value shall be between 30 kHz and 33 kHz products.

Possible Problems:

Some products may not support disconnect during the process of enabling BIST and testing. For these products, refer to the Disconnect sections of reference [5] for setup requirement.

Test PHY-04 - Spread-Spectrum Modulation Deviation

Purpose: To verify that the Spread-Spectrum Modulation Deviation of the Products Under Test's (PUT's) transmitter is within the conformance limits.

References:

[1] Serial ATA Revision 3.0, 7.2.1, Table 29 – General Specifications
[2] Ibid, 7.2.2.1.6 and 7.3.3 – Spread-Spectrum Modulation Deviation
[3] Ibid, 7.4.14 – SSC Profile
[4] SATA Interoperability Program Unified Test Document, 2.13.4 – Spread-Spectrum Modulation Deviation
[5] Pre-Test MOI

Resource Requirements:

Same requirements as for PHY-01

Last Template Modification: May 3, 2013 (Version 1.65)

Discussion:

Reference [1] specifies the general PHY conformance limits for SATA products. This specification includes conformance limits for the Spread-Spectrum Modulation Deviation. Reference [2] provides the definition of this term for the purposes of SATA testing. Reference [3] defines the measurement requirements for this test.

In this test, the Spread-Spectrum Modulation Deviation is measured, based on at least 10 complete SSC cycles.

This test is only run once at the maximum interface rate of the product (1.5Gb/s, 3.0Gb/s or 6.0Gb/s)

Test Setup:

Same setup as for PHY-01.

Test Procedure:

This parameter is covered by Keysight Technologies, Inc. N5411B (legacy solution) AND D9030SATC (current solution nomenclature) automated SATA compliance software, revision 1.65 or later. The Max Unit Interval is measured over the entire trend and converted to ppm deviation. The Min Unit Interval is measured over the entire trend and converted to ppm. Both Max and Min UI must be within the limits of the specification to pass this test. Either "PASS" or "FAIL" is shown for the SSC modulation deviation test in the report generated at the completion of the testing.

The measurement for SSC modulation deviation records the mean of max unit interval values after the 1.98MHz filter is applied. The value reported as the result must be the single total range value relative to nominal of the SSC modulation deviation, using the equations below, where "Min" is the mean of 10 recorded values of the minimum peaks and "Max: is the mean of 10 recorded values of the maximum peaks. The ppm deviation is computed from the following operations and compared against spec value for pass/fail:

Calculate max deviation = (Measured Max – Nominal)/Nominal * 1e6 ppm
Calculate min deviation = (Measured Min – Nominal)/Nominal * 1e6 ppm

Nominal is defined as 666.6667ps for Gen 1 MAX data rate products, 333.3333ps for Gen 2 MAX data rate products and 166.6667ps for Gen3 MAX data rate products.

Observable Results:

a) Max SSC_{tol} measured (using mean of 10 recorded values) less than +350ppm.
b) Min SSC_{tol} measured (using mean of 10 recorded values) greater than -5350ppm.

Possible Problems:

Some products may not support disconnect during the process of enabling BIST and testing. For these products, refer to the Disconnect sections of reference [5] for setup requirement.

PHY TRANSMIT SIGNAL REQUIREMENTS

Overview:

This group of tests verifies the Phy Transmitted Signal Requirements, as defined in Section 2.15 of the Serial ATA Interoperability Unified Test Document, Revision 1.6 (which references Serial ATA Revision 3.4).

Test TSG-01 - Differential Output Voltage

Purpose: To verify that the Differential Output Voltage of the Products Under Test's (PUT's) transmitter is within the conformance limits.

References:

[1] Serial ATA Revision 3.0, 7.2.1, Table 31 – Transmitted Signal Requirements
[2] Ibid, 7.2.2.2.7 – TX Differential Output Voltage
[3] Ibid, 7.4. 5 – Transmitter Amplitude
[4] SATA Interoperability Program Unified Test Document, 2.15.1 – Differential Output Voltage
[5] Pre-Test MOI

Resource Requirements:

Same as for PHY-01, repeated here for convenience:

- Keysight DSAX93204A, DSAX92804A, DSAX92504A, DSAX92004A and DSAX91604A (32GHz, 28GHz, 25GHz, 20GHz and 16GHz bandwidth, 80GS/s per channel) or Keysight DSA91204A (12GHz bandwidth, 40GS/s per channel)
- Keysight N5411B (legacy solution) AND D9030SATC (current solution nomenclature) SATA 6 Gb/s Compliance Test Software
- Wilder Technologies SATA Gen3 Receptacle Adapter SATA-TPA-R or ICT-Lanto SATA Receptacle Gen 3 TF-1R31 or Crescent Heart Software TF-SATA-NE/ZP or TF-eSATA-NE/ZP test adapter or equivalent
- Keysight N4903B J-BERT (with Option 002), Gen2i capable products PC running ULink, SerialTek BusMod BusGen BIST Generator or any other mechanism that makes the products produce the required patterns is acceptable.

See appendix A for details.

Last Template Modification: May 3, 2013 (Version 1.65)

Discussion:

Reference [1] specifies the Transmitted Signal conformance limits for SATA products. This specification includes conformance limits for the Differential Output Voltage. Reference [2] provides the definition of this term for the purposes of SATA testing. Reference [3] defines the measurement requirements for this test.

Vdiff Min is tested with HFTP, MFTP and LBP. Vdiff Max is tested with MFTP and LFTP.

For products which support 3Gb/s or 6Gb/s, this requirement must be tested at both 1.5Gb/s and 3.0Gb/s interface rates. Separate tests for 6Gb/s Max Amplitude and 6Gb/s Min Amplitude are defined in TSG-014 and TSG-015, respectively.

Test Setup:

1. Since PHY-01 the products has been producing HFTP and it is already connected to the scope. The N5411B (legacy solution) AND D9030SATC (current solution nomenclature) SATA compliance software will prompt for MFTP, LBP and LFTP when it needs those patterns. When prompted, follow the procedures in reference [5] to activate those BIST-TAS patterns. Or keep products in BIST-L.

2. Plug the test fixture into the products. The test fixture is connected to channels 1 and 3 of the scope by two 36" SMA cables (Rosenberger or equivalent). OBSERVE the signal on the scope. If it is correct, press OK in the N5411B (legacy solution) AND D9030SATC (current solution nomenclature) prompt. If not, the products did not properly handle BIST Activate FIS; a non-standard way to make it produce the desired pattern will be required.

Test Procedure:

This parameter is covered by Keysight Technologies, Inc. N5411B (legacy solution) AND D9030SATC (current solution nomenclature) automated SATA compliance software, revision 1.65 or later. Interim values for UH (HFTP upper), LH (HFTP lower), UM (MFTP upper), LM (MFTP lower), DHM (worst-case differential HFTP or differential MFTP), A (LBP lone 1-bit upper) and B (LBP lone 0-bit lower) are measured and computed to determine the final Vtest value for the Minimum Amplitude test. These interim values and screen captures can also be a helpful aid in debugging which pattern, and specifically, which bit failed the test. Similar steps are used to setup the MFTP and LFTP patterns used for the Maximum Amplitude test.

NOTE: The N5411B (legacy solution) AND D9030SATC (current solution nomenclature) maximum amplitude test does not test physical voltage, but instead, the ratio of amplitude histogram points at or above the physical specification limit compared to total amplitude histogram points at or above +/- DOV/2. Again, pu, nu, NU, pl, nl and NL are reported out to assist in debug. This methodology is provided per the VdiffTX, Max measurement definition in reference [1]. Either "PASS" or "FAIL" is shown for the minimum amplitude test in the report generated at the completion of the testing.

Reference [4] addresses the measurement of VdiffTX, Min per the SATA-IO LOGO IW testing requirements as follows:

DOV Min = Vtest(min) = min(DH, DM, VtestLBP)

Observable Results:

The Differential Output Voltage shall be between the limits specified in reference [4]. For convenience, the values are reproduced below. For the differential amplitude voltage test to pass, the minimum differential amplitude value, Vtest(min), must meet the DOV minimum test limits. Measurements for pu and pl should be recorded as well but are informative only.

PUT Type	DOV Min
Gen1i	400 mV
Gen2i	400 mV

Possible Problems:

Some products may not support disconnect during the process of enabling BIST and testing. For these products, refer to the Disconnect sections of reference [5] for setup requirement.

Test TSG-02 - Rise/Fall Time (Informative)

Purpose: To verify that the Rise/Fall time of the Products Under Test's (PUT's) is within the conformance limits.

References:

[1] Serial ATA Revision 3.0, 7.2.1, Table 31 – Transmitted Signal Requirements
[2] Ibid, 7.2.2.2.9 – TX Rise/Fall Time
[3] Ibid, 7.4.4 – Rise and Fall Times
[4] SATA Interoperability Program Unified Test Document, 2.15.2 – Rise/Fall Time
[5] Pre-Test MOI

Resource Requirements:

Same as for TSG-01.

See appendix A for details.

Last Template Modification: May 3, 2013 (Version 1.65)

Discussion:

Reference [1] specifies the Transmitted Signal conformance limits for SATA products. This specification includes conformance limits for the Rise/Fall Time. Reference [2] provides the definition of this term for the purposes of SATA testing. Reference [3] defines the measurement requirements for this test.

TSG-02 is tested using LFTP. For products which support 3Gb/s or 6Gb/s, this requirement must be tested at both 1.5Gb/s and 3.0Gb/s interface rates.

The cables connecting the Wilder Technologies SATA Gen3 Receptacle Adapter SATA-TPA-R or ICT-Lanto SATA Receptacle Gen 3 TF-1R31 or Crescent Heart Software TF-SATA-NE/ZP or TF-eSATA-NE/ZP test adapter or equivalent to the scope must be deskewed, as discussed in Appendix A. Skew lengthens the measured differential rise and fall times.

Test Setup:

1. The N5411B (legacy solution) AND D9030SATC (current solution nomenclature) SATA compliance software will prompt for LFTP when it needs that pattern. When prompted, follow the procedures in reference [5] to enable BIST-TAS LFTP. Or keep products in BIST-L.

2. Plug the test fixture into the products. The test fixture is connected to channels 1 and 3 of the scope by two 36" SMA cables (Rosenberger or equivalent). OBSERVE the signal on the scope. If it is LFTP, press OK in the N5411B (legacy solution) AND D9030SATC (current solution nomenclature) prompt. If not, the products did not properly handle BIST Activate FIS; a non-standard way to make it produce the desired pattern will be required.

Test Procedure:

This parameter is covered by Keysight Technologies, Inc. N5411B (legacy solution) AND D9030SATC (current solution nomenclature) automated SATA compliance software, revision 1.65 or later. The Mean value is reported as the final value and compared only to the RFT Max value in the table below for pass/fail. Either "PASS" or "FAIL" is shown for the Rise/Fall time test in the report generated at the completion of the testing.

Observable Results:

The Mean TX Rise/Fall Times shall be between the limits specified in reference [1]. For convenience, the values are reproduced below. Note: Failures of minimum rise and fall time limits have not been shown to affect interoperability and will not be included in determining pass/fail for Interoperability testing.

Limit	Time @ 1.5Gb/s (ps (UI))	Time @ 3Gb/s (ps (UI))	Time @ 6Gb/s (ps (UI))
Min 20-80%	100 (0.15)	67 (0.20)	33 (0.20)

Max 20-80%	273 (0.41)	136 (0.41)	68 (0.41)

Possible Problems:

Some products may not support disconnect during the process of enabling BIST and testing. For these products, refer to the Disconnect sections of reference [5] for setup requirement.

Test TSG-03 - Differential Skew (Informative)

Purpose: To verify that the Differential Skew of the Products Under Test's (PUT's) transmitter is within the conformance limits.

References:

[1] Serial ATA Revision 3.0, 7.2.1, Table 31 – Transmitted Signal Requirements
[2] Ibid, 7.2.2.2.10 – TX Differential Skew (Gen2i, Gen1x, Gen2x)
[3] Ibid, 7.4.15 – Intra-pair Skew
[4] SATA Interoperability Program Unified Test Document, 2.15.3 – Differential Skew
[5] Pre-Test MOI

Resource Requirements:

Same as for TSG-01.

See appendix A for details.

Last Template Modification: May 3, 2013 (Version 1.65)

Discussion:

Reference [1] specifies the Transmitted Signal conformance limits for SATA products. This specification includes conformance limits for Differential Skew. Reference [2] provides the definition of this term for the purposes of SATA testing. Reference [3] defines the measurement requirements for this test.

Skew is measured with HFTP and MFTP. This test is only run once at the maximum interface rate of the product (1.5Gbps or 3.0Gbps).

The cables connecting the Wilder Technologies SATA Gen3 Receptacle Adapter SATA-TPA-R or ICT-Lanto SATA Receptacle Gen 3 TF-1R31 or Crescent Heart Software TF-SATA-NE/ZP or TF-eSATA-NE/ZP test adapter or equivalent to the scope must be deskewed, as discussed in Appendix A. Uncompensated cable skew contributes directly to measured differential skew.

Test Setup:

1. The N5411B (legacy solution) AND D9030SATC (current solution nomenclature) SATA compliance software will prompt for HFTP and MFTP when it needs those patterns. When prompted follow the procedures in reference [5] to enable those BIST-TAS patterns. Or keep products in BIST-L.

2. Plug the test fixture to products. The test fixture is connected to channels 1 and 3 of the scope by two 36" SMA cables (Rosenberger or equivalent). OBSERVE the signal on the scope. If it is the correct pattern, press OK in the N5411B (legacy solution) AND D9030SATC (current solution nomenclature) prompt. If not, the products did not properly handle BIST Activate FIS; a non-standard way to make it produce the desired pattern will be required.

Test Procedure:

This parameter is covered by Keysight Technologies, Inc. N5411B (legacy solution) AND D9030SATC (current solution nomenclature) automated SATA compliance software, revision 1.65 or later. This requires measuring the mean skew of TX+ rise mid-point to the TX- fall mid-point and the mean skew of TX+ fall mid-point to TX- rise mid-point, and finally computing the Differential Skew = average of the magnitude (absolute value) of the two mean skews. This removes the effect of rise-fall imbalance from the skew measurement. Two differential skew values are provided, one for HFTP and one for MFTP, and both must meet the Max Diff Skew requirements in reference [1], which are repeated in the table below for convenience. Either "PASS" or "FAIL" is shown for the differential skew test in the report generated at the completion of the testing.

Observable Results:

The TX Differential Skew shall be between the limits specified in reference [1]. For convenience, the values are reproduced below.

PUT Type	Max Diff Skew
Gen1i	20 ps
Gen2i	20 ps

Possible Problems:

Some products may not support disconnect during the process of enabling BIST and testing. For these products, refer to the Disconnect sections of reference [5] for setup requirement.

Test TSG-04 - AC Common Mode Voltage

Purpose: To verify that the AC Common Mode Voltage of the Products Under Test's (PUT's) transmitter is within the conformance limits.

References:

[1] Serial ATA Revision 3.0, 7.2.1, Table 31 – Transmitted Signal Requirements
[2] Ibid, 7.2.2.2.11 – TX AC Common Mode Voltage (Gen2i, Gen1x, Gen2x)
[3] Ibid, 7.4.20 – TX AC Common Mode Voltage
[4] SATA Interoperability Program Unified Test Document, 2.15.4 – AC Common Mode Voltage
[5] Pre-Test MOI

Resource Requirements:

Same as for TSG-01.

See appendix A for details.

Last Template Modification: May 3, 2013 (Version 1.65)

Discussion:

Reference [1] specifies the Transmitted Signal conformance limits for SATA products. This specification includes conformance limits for the TX AC Common Mode Voltage. Reference [2] provides the definition of this term for the purposes of SATA testing. Reference [3] defines the measurement requirements for this test.

MFTP is required for Gen1u, Gen2u, Gen2i Gen2m, Gen3i, Gen3u. Additional HFTP is required for Gen1u, Gen2u, Gen3i, Gen3u. The analysis bandwidth shall be limited by a band pass filter with a low frequency cutoff at 200 MHz and a high frequency cutoff of Fbaud/2 (fundamental frequency of the data rate) with a 1st order filter roll off response. The measurement should also be done with at least 10,000 UIs.

The cables connecting the Wilder Technologies SATA Gen3 Receptacle Adapter SATA-TPA-R or ICT-Lanto SATA Receptacle Gen 3 TF-1R31 or Crescent Heart Software TF-SATA-NE/ZP or TF-eSATA-NE/ZP test adapter or equivalent to the scope must be deskewed, as discussed in Appendix A. Skew contributes directly to common mode spikes which if large enough, even though they are low pass filtered to half the bit rate, can cause failure.

Test Setup:

1. The N5411B (legacy solution) AND D9030SATC (current solution nomenclature) SATA compliance software will prompt for MFTP. When prompted for MFTP, follow the procedures in reference [5] to enable BIST-TAS MFTP. Or keep products in BIST-L.

2. Plug the test fixture into the products. The test fixture is connected to channels 1 and 3 of the scope by two 36" SMA cables (Rosenberger or equivalent). OBSERVE the signal on the scope. If it is MFTP, press OK in the N5411B (legacy solution) AND D9030SATC (current solution nomenclature) prompt. If not, the products did not properly handle BIST Activate FIS; a non-standard way to make it produce the desired pattern will be required.

Test Procedure:

This parameter is covered by Keysight Technologies, Inc. N5411B (legacy solution) AND D9030SATC (current solution nomenclature) automated SATA compliance software, revision 1.65 or later. The test is performed as (TX+ + TX-)/2, band pass filter applied with a low frequency cutoff at 200 MHz and a high frequency cutoff of Fbaud/2 (fundamental frequency of the data rate) with a 1st order filter roll off response and peak-peak amplitude of the filter output measured as the final AC common mode voltage value. Either "PASS" or "FAIL" is shown for the common mode voltage test in the report generated at the completion of the testing.

Observable Results:

The AC Common Mode Voltage value shall be less than 50 mVp-p (Gen2i, Gen2u), 100 mVp-p (Gen1u, Gen2u) and 120 mVp-p (Gen3i, Gen3u) products.

Possible Problems:

Please see TSG-03.

Test TSG-05 - Rise/Fall Imbalance (Obsolete)

Purpose: To verify that the Rise/Fall Imbalance of the Product Under Test's (PUT's) transmitter is within the conformance limits.

References:

[1] Serial ATA Revision 3.0, 7.2.1, Table 31 – Transmitted Signal Requirements
[2] Ibid, 7.2.22.16 – TX Rise/Fall Imbalance
[3] Ibid, 7.4.19 – TX Rise/Fall Imbalance
[4] SATA Interoperability Program Unified Test Document, 2.15.5 – Rise/Fall Imbalance
[5] Pre-Test MOI

Resource Requirements:

Same as for TSG-01.

See appendix A for details.

Last Template Modification: May 3, 2013 (Version 1.65)

Discussion:

Reference [1] specifies the Transmitted Signal conformance limits for SATA products. This specification includes conformance limits for the Rise/Fall Imbalance. Reference [2] provides the definition of this term for the purposes of SATA testing. Reference [3] defines the measurement requirements for this test.

Rise/Fall imbalance is measured with LFTP. References [2] and [3] both define two values to be computed, for each pattern. The two values compare TX+ rise to TX- fall, and TX- rise to TX+ fall. The results are expressed as a percentage of the worst case of the two items being compared. The MEAN R/F Imbalance is reported as the final result. This test requirement is only applicable to products running at 3Gbps.

Test Setup:

1. The N5411B (legacy solution) AND D9030SATC (current solution nomenclature) SATA compliance software will prompt for LFTP when it needs those patterns. When prompted, follow the procedures in reference [5] to enable those BIST-TAS patterns. Or keep the products in BIST-L.

2. Plug the test fixture into the products. The test fixture is connected to channels 1 and 3 of the scope by two 36" SMA cables (Rosenberger or equivalent). OBSERVE the signal on the scope. If it is correct, press OK in the N5411B (legacy solution) AND D9030SATC (current solution nomenclature) prompt. If not, the products did not properly handle BIST Activate FIS; a non-standard way to make it produce the desired pattern will be required.

Test Procedure:

This parameter is covered by Keysight Technologies, Inc. N5411B (legacy solution) AND D9030SATC (current solution nomenclature) automated SATA compliance software, revision 1.65 or later. Either "PASS" or "FAIL" is shown for the rise/fall imbalance test in the report generated at the completion of the testing.

Observable Results:

The Rise/Fall Imbalance value shall be less than 20% for Gen2i and Gen2m products.

Possible Problems:

Some products may not support disconnect during the process of enabling BIST and testing. For these products, refer to the Disconnect sections of reference [5] for setup requirement.

Test TSG-06 - Amplitude Imbalance (Obsolete)

Purpose: To verify that the Amplitude Imbalance of the Products Under Test's (PUT's) transmitter is within the conformance limits.

References:

[1] Serial ATA Revision 3.0, 7.2.1, Table 31 – Transmitted Signal Requirements
[2] Ibid, 7.2.2.2.17 – TX Amplitude Imbalance (Gen2i, Gen1x, Gen2x)
[3] Ibid, 7.4.18 – TX Amplitude Imbalance
[4] SATA Interoperability Program Unified Test Document, 2.15.6 – Amplitude Imbalance
[5] Pre-Test MOI

Resource Requirements:

Same as for TSG-01.

See appendix A for details.

Last Template Modification: May 3, 2013 (Version 1.65)

Discussion:

Reference [1] specifies the Transmitted Signal conformance limits for SATA products. This specification includes conformance limits for the TX Amplitude Imbalance. Reference [2] provides the definition of this term for the purposes of SATA testing. Reference [3] defines the measurement requirements for this test.

Amplitude Imbalance is measured with HFTP and MFTP. This test requirement is only applicable to products running at 3Gbps.

This parameter is a measure of the match in the single-ended amplitudes of the TX+ and TX- signals. This parameter shall be measured and met with both the HFTP and MFTP patterns. Clock-like patterns are used here to enable the use of standard mode-based amplitude measurements for the sole purpose of determining imbalance. Due to characteristics of the MFTP, it is required that the measurement points be taken at 0.5UI of the 2nd bit within the pattern. All amplitude values for this measurement shall be the statistical mode measured at 0.5UI nominal over a minimum of 10,000UI. The amplitude imbalance value for each pattern is then determined by the equation:

absolute value(TX+ amplitude - TX- amplitude) / ((TX+ amplitude + TX- amplitude)/2)

Test Setup:

1. The N5411B (legacy solution) AND D9030SATC (current solution nomenclature) SATA compliance software will prompt for HFTP and MFTP when it needs those patterns. When prompted, follow the procedures in reference [5] to enable those BIST-TAS patterns. Or keep products in BIST-L.

2. Plug the test fixture into the products. The test fixture is connected to channels 1 and 3 of the scope by two 36" SMA cables (Rosenberger or equivalent). OBSERVE the signal on the scope. If it is correct, press OK in the N5411B (legacy solution) AND D9030SATC (current solution nomenclature) prompt. If not, the products did not properly handle BIST Activate FIS; a non-standard way to make it produce the desired pattern will be required.

Test Procedure:

This parameter is covered by Keysight Technologies, Inc. N5411B (legacy solution) AND D9030SATC (current solution nomenclature) automated SATA compliance software, revision 1.65 or later. Either "PASS" or "FAIL" is shown for the rise/fall imbalance test in the report generated at the completion of the testing.

Observable Results:

The TX Amplitude Imbalance value shall be less than 10% for Gen1x, Gen2i, Gen2m, and Gen2x products.

Possible Problems:

Some products may not support disconnect during the process of enabling BIST and testing. For these products, refer to the Disconnect sections of reference [5] for setup requirement.

Test TSG-07 - Gen1 (1.5Gbps) TJ at Connector, Clock to Data, Fbaud/10 (Obsolete)

Note: This test is no longer required. It has been left here only for historical reference.

Purpose: Data-to-Data jitter is a measure of variance in the zero crossing times of edges at a fixed time (t_n) equal to an integer number of Unit intervals (n) after triggering on data edges (t_0). Since t_0 is triggered from the serial signal rather than a Reference Clock the resulting measurements do represent a combination of the jitter at t_0 and t_n.

References:

[1] SATA Interoperability Program Unified Test Document, 2.15.7 – TJ at Connector, Clock to Data, Fbaud/10

Resource Requirements:

Same as for TSG-01.

Last Template Modification: May 3, 2013 (Version 1.65)

Discussion:

This measurement is no longer defined in Serial ATA Revision 3.2 and later.

Test TSG-08 - Gen1 (1.5Gbps) DJ at Connector, Clock to Data, Fbaud/10 (Obsolete)

Note: This test is no longer required. It has been left here only for historical reference.

Purpose: Data-to-Data jitter is a measure of variance in the zero crossing times of edges at a fixed time (t_n) equal to an integer number of Unit intervals (n) after triggering on data edges (t_0). Since t_0 is triggered from the serial signal rather than a Reference Clock the resulting measurements do represent a combination of the jitter at t_0 and t_n.

References:

[1] SATA Interoperability Program Unified Test Document, 2.15.8 – DJ at Connector, Clock to Data, Fbaud/10

Resource Requirements:

Same as for TSG-01.

Last Template Modification: May 3, 2013 (Version 1.65)

Discussion:

This measurement is no longer defined in Serial ATA Revision 3.0 and later.

Test TSG-09 - Gen1 (1.5Gbps) TJ at Connector, Clock to Data, Fbaud/500 (JTF Defined)

Purpose: To verify that the TJ at Connector (Clock to Data, Fbaud/500) of the Product Under Test's (PUT's) transmitter is within the conformance limits.

References:

[1] Serial ATA Revision 3.0, 7.2.1, Table 31 – Transmitted Signal Requirements
[2] Ibid, 7.2.2.2.18
[3] Ibid, 7.3.2, 7.4.8
[4] SATA Interoperability Program Unified Test Document, 2.15.9 – TJ at Connector, Clock to Data, Fbaud/500
[5] Pre-Test MOI

Resource Requirements:

Same as for TSG-01.

See appendix A for details.

Last Template Modification: May 3, 2013 (Version 1.65)

Discussion:

Reference [1] specifies the Transmitted Signal conformance limits for SATA products. This specification includes conformance limits for the TJ at Connector (Clock, 500). Reference [2] provides the definition of this term for the purposes of SATA testing. Reference [3] defines the measurement requirements for this test.

For products which support 3Gb/s or 6Gb/s, this requirement must be tested at 1.5Gb/s.

For the Integrator's List test program jitter measurements are required to be made with HFTP and LBP, and optionally with SSOP.

Test Setup:

1. The N5411B (legacy solution) AND D9030SATC (current solution nomenclature) SATA compliance software will prompt for HFTP, LBP and/or SSOP when it needs those patterns. When prompted, follow the procedures in reference [5] to enable those BIST-TAS patterns. Or keep products in BIST-L.

2. Plug the test fixture into the products. The test fixture is connected to channels 1 and 3 of the scope by two 36" SMA cables (Rosenberger or equivalent). OBSERVE the signal on the scope. If it is correct, press OK in the N5411B (legacy solution) AND D9030SATC (current solution nomenclature) prompt. If not, the products did not properly handle BIST Activate FIS; a non-standard way to make it produce the desired pattern will be required.

Test Procedure:

This parameter is covered by Keysight Technologies, Inc. N5411B (legacy solution) AND D9030SATC (current solution nomenclature) automated SATA compliance software, revision 1.65 or later. Either "PASS" or "FAIL" is shown for the Gen II TJ test in the report generated at the completion of the testing.

Observable Results:

The TJ shall be less than 0.37UI for Gen1 products.

Possible Problems:

Some products may not support disconnect during the process of enabling BIST and testing. For these products, refer to the Disconnect sections of reference [5] for setup requirement.

Test TSG-10 - Gen1 (1.5Gbps) DJ at Connector, Clock to Data, Fbaud/500 (JTF Defined)

Purpose: To verify that the DJ at Connector (Clock to Data, Fbaud/500) of the Product Under Test's (PUT's) transmitter is within the conformance limits.

References:

[1] Serial ATA Revision 3.0, 7.2.1, Table 31 – Transmitted Signal Requirements
[2] Ibid, 7.2.2.2.18
[3] Ibid, 7.3.2, 7.4.8
[4] SATA Interoperability Program Unified Test Document, 2.15.10 – DJ at Connector, Clock to Data, Fbaud/500
[5] Pre-Test MOI

Resource Requirements:

Same as for TSG-01.

See appendix A for details.

Last Template Modification: May 3, 2013 (Version 1.65)

Discussion:

Reference [1] specifies the Transmitted Signal conformance limits for SATA products. This specification includes conformance limits for the DJ at Connector (Clock to Data, Fbaud/500). Reference [2] provides the definition of this term for the purposes of SATA testing. Reference [3] defines the measurement requirements for this test.

For products which support 3Gb/s or 6Gb/s, this requirement must be tested at 1.5Gb/s.

For the Integrator's List test program jitter measurements are required to be made with HFTP and LBP, and optionally with SSOP.

Test Setup:

This test result is derived at the same time as TSG-09. Therefore, no setup change is needed for TSG-10.

Test Procedure:

This parameter is covered by Keysight Technologies, Inc. N5411B (legacy solution) AND D9030SATC (current solution nomenclature) automated SATA compliance software, revision 1.65 or later. Either "PASS" or "FAIL" is shown for the Gen II TJ test in the report generated at the completion of the testing.

Observable Results:

The DJ shall be less than 0.19UI for Gen1 products.

Possible Problems:

Some products may not support disconnect during the process of enabling BIST and testing. For these products, refer to the Disconnect sections of reference [5] for setup requirement.

Test TSG-11 - Gen2 (3.0Gbps) TJ at Connector, Clock to Data, Fbaud/500 (JTF Defined)

Purpose: To verify that the TJ at Connector (Clock, 500) of the Product Under Test's (PUT's) transmitter is within the conformance limits.

References:

[1] Serial ATA Revision 3.0, 7.2.1, Table 31 – Transmitted Signal Requirements
[2] Ibid, 7.2.2.2.18
[3] Ibid, 7.3.2, 7.4.8
[4] SATA Interoperability Program Unified Test Document, 2.15.11 – TJ at Connector, Clock to Data, Fbaud/500
[5] Pre-Test MOI

Resource Requirements:

Same as for TSG-01

See appendix A for details.

Last Template Modification: May 3, 2013 (Version 1.65)

Discussion:

Reference [1] specifies the Transmitted Signal conformance limits for SATA products. This specification includes conformance limits for the TJ at Connector (Clock to data, Fbaud/500). Reference [2] provides the definition of this term for the purposes of SATA testing. Reference [3] defines the measurement requirements for this test.

For products which support 3Gb/s or 6Gb/s, this requirement must be tested at 3Gb/s.

For the Integrator's List test program jitter measurements are required to be made with HFTP and LBP, and optionally with SSOP.

Test Setup:

1. The N5411B (legacy solution) AND D9030SATC (current solution nomenclature) SATA compliance software will prompt for HFTP, LBP and/or SSOP when it needs those patterns. When prompted, follow the procedures in reference [5] to enable those BIST-TAS patterns. Or keep products in BIST-L.

2. Plug the test fixture into the products. The test fixture is connected to channels 1 and 3 of the scope by two 36" SMA cables (Rosenberger or equivalent). OBSERVE the signal on the scope. If it is correct, press OK in the N5411B (legacy solution) AND D9030SATC (current solution nomenclature) prompt. If not, the products did not properly handle BIST Activate FIS; a non-standard way to make it produce the desired pattern will be required.

Test Procedure:

This parameter is covered by Keysight Technologies, Inc. N5411B (legacy solution) AND D9030SATC (current solution nomenclature) automated SATA compliance software, revision 1.65 or later. Either "PASS" or "FAIL" is shown for the Gen II TJ test in the report generated at the completion of the testing.

Observable Results:

The TJ shall be less than 0.37UI for 3.0Gb/s products.

Possible Problems:

Some products may not support disconnect during the process of enabling BIST and testing. For these products, refer to the Disconnect sections of reference [5] for setup requirement.

Test TSG-12 - Gen2 (3.0Gbps) DJ at Connector, Clock to Data, Fbaud/500 (JTF Defined)

Purpose: To verify that the DJ at Connector (Clock, 500) of the Product Under Test's (PUT's) transmitter is within the conformance limits.

References:

[1] Serial ATA Revision 3.0, 7.2.1, Table 31 – Transmitted Signal Requirements
[2] Ibid, 7.2.2.2.18
[3] Ibid, 7.3.2, 7.4.8
[4] SATA Interoperability Program Unified Test Document, 2.15.12 – DJ at Connector, Clock to data, Fbaud/500
[5] Pre-Test MOI

Resource Requirements:

Same as for TSG-01.

See appendix A for details.

Last Template Modification: May 3, 2013 (Version 1.65)

Discussion:

Reference [1] specifies the Transmitted Signal conformance limits for SATA products. This specification includes conformance limits for the DJ at Connector (Clock to Data, Fbaud/500). Reference [2] provides the definition of this term for the purposes of SATA testing. Reference [3] defines the measurement requirements for this test.

For products which support 3Gb/s or 6Gb/s, this requirement must be tested at 3Gb/s.

For the Integrator's List test program jitter measurements are required to be made with HFTP and LBP, and optionally with SSOP.

Test Setup:

This test result is derived at the same time as TSG-11. Therefore, no setup change is needed for TSG-12.

Test Procedure:

This parameter is covered by Keysight Technologies, Inc. N5411B (legacy solution) AND D9030SATC (current solution nomenclature) automated SATA compliance software, revision 1.65 or later. Either "PASS" or "FAIL" is shown for the Gen II TJ test in the report generated at the completion of the testing.

Observable Results:

The DJ shall be less than 0.19UI when measured at $f_{BAUD}/500$ for Gen2 products.

Possible Problems:

Some products may not support disconnect during the process of enabling BIST and testing. For these products, refer to the Disconnect sections of reference [5] for setup requirement.

Test TSG-13 - Gen3 (6.0Gbps) Transmit Jitter before and after CIC, Clock to Data (JTF Defined)

Purpose: To verify that the TJ of the product's transmitter is within the conformance limits, both at the near-end connector compliance point and at the far-end of the Compliance Interconnect Channel (CIC).

References:

[1] Serial ATA Revision 3.0, 7.2.1, Table 31 – Transmitted Signal Requirements
[2] Ibid, 7.2.2.2.18
[3] Ibid, 7.3.2.4, 7.4.8, 7.4.10
[4] SATA Interoperability Program Unified Test Document, 2.15.13 – Gen3 (6Gb/s) Transmit Jitter
[5] Pre-Test MOI

Resource Requirements:

Same as for TSG-01.

See appendix A for details.

Last Template Modification: May 3, 2013 (Version 1.65)

Discussion:

Reference [1] specifies the Transmitted Signal conformance limits for SATA products. This specification includes conformance limits for the TJ both at the near-end connector compliance point and at the far-end of the compliance Interconnect Channel (CIC). Reference [2] provides the definition of this term for the purposes of SATA testing. Reference [3] defines the measurement requirements for this test.

This test requirement is only applicable to products running at 6Gb/s.

For the Integrator's List test program jitter measurements are required to be made with HFTP, MFTP, LFTP, SSOP and LBP. RJ is measured as an RMS value directly from the transmitter connector (compliance interface) into a laboratory load using the MFTP pattern. SATA ECN-39 outlines modified provision to TSG-13 where TJ peak-to-peak value at BER levels of 10E-6 and 10E-12 are evaluated. The Compliance Interconnect Channel for this test is implemented as a frequency-domain filter created from the standard SATA_CIC_Spec.s4p file, which includes both frequency and phase information as measured directly from the hardware CIC model defined in [1]. Implementation of the CIC in this fashion allows for no disruption of the laboratory load connection during jitter testing, and prevents the addition of additional cabling loss between the product under test and the laboratory load. For a Gen3u UHost PUT, the Gen3i CIC channel is not used and the measurement is made directly into the lab load. Additionally reference Table 38 (General Electrical) for Gen1u, Gen2u, Gen3u Host based on electrical specifications.

Test Setup:

1. The N5411B (legacy solution) AND D9030SATC (current solution nomenclature) SATA compliance software will prompt for LBP. When prompted, follow the procedures in reference [5] to enable those BIST-TAS patterns. Or keep products in BIST-L.

2. Plug the test fixture into the products. The test fixture is connected to channels 1 and 3 of the scope by two 36" SMA cables (Rosenberger or equivalent). OBSERVE the signal on the scope. If it is correct, press OK in the N5411B (legacy solution) AND D9030SATC (current solution nomenclature) prompt. If not, the products did not properly handle BIST Activate FIS; a non-standard way to make it produce the desired pattern will be required.

Test Procedure:

This parameter is covered by Keysight Technologies, Inc. N5411B (legacy solution) AND D9030SATC (current solution nomenclature) automated SATA compliance software, revision 1.65 or later. Either "PASS" or "FAIL" is shown for the 6Gb/s TJ test in the report generated at the completion of the testing.

Observable Results:

- TJ (BER of 1E-12) measured at a maximum of 0.52 UI into a Laboratory Load after the CIC (for Gen3i PUT) or without the CIC (for Gen3u UHost PUT) using the specified JTF (for products running at 6Gb/s)
- • TJ (BER of 1E-6) measured at a maximum of 0.46 UI into a Laboratory Load after the CIC (for Gen3i PUT) or without the CIC (for Gen3u UHost PUT) using the specified JTF (for products running at 6Gb/s)

Possible Problems:

Some products may not support disconnect during the process of enabling BIST and testing. For these products, refer to the Disconnect sections of reference [5] for setup requirement.

Test TSG-14 - Gen3 (6.0Gbps) Transmitter Maximum Differential Voltage Amplitude

Purpose: To verify that the Maximum Amplitude of the product's transmitter is within the conformance limits.

References:

[1] Serial ATA Revision 3.0, 7.2.1, Table 31 – Transmitted Signal Requirements
[2] Ibid, 7.2.2.2.7
[3] Ibid, 7.4.3, 7.4.5
[4] SATA Interoperability Program Unified Test Document, 2.15.14 – Gen3 (6Gb/s) Maximum Differential Voltage Amplitude
[5] Pre-Test MOI

Resource Requirements:

Same as for TSG-01.

See appendix A for details.

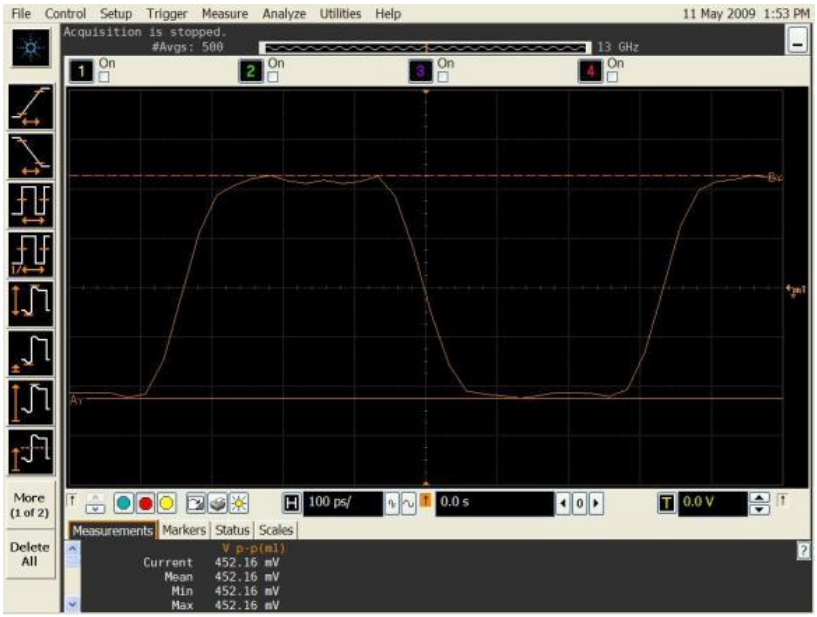
Last Template Modification: May 3, 2013 (Version 1.65)

Discussion:

Reference [1] specifies the Transmitted Signal conformance limits for SATA products. The maximum differential amplitude shall be measured at the TX Compliance point into a Lab Load. A Gen3 MFTP shall be used for this compliance measurement. The MFTP will contain emphasis due to its run length, if the transmitter supports this signal conditioning, and allows for simple edge triggering for the signal capture.

The maximum amplitude is defined as the peak to peak value of the average of 500 waveforms measured over a time span of 4 Gen3 UI, using the HBWS. Reference [2] provides the definition of this term for the purposes of SATA testing. Reference [3] defines the measurement requirements for this test.

This test requirement is only applicable to products running at 6Gb/s.



Peak-to-Peak Voltage Measurement of 500 Time-Averaged acquisitions of 4 consecutive MFTP UI

Test Setup:

1. The N5411B (legacy solution) AND D9030SATC (current solution nomenclature) SATA compliance software will prompt for MFTP when needed. When prompted, follow the procedures in reference [5] to enable those BIST-TAS patterns. Or keep products in BIST-L.

2. Plug the test fixture into the products. The test fixture is connected to channels 1 and 3 of the scope by two 36" SMA cables (Rosenberger or equivalent). OBSERVE the signal on the scope. If it is correct, press OK in the N5411B (legacy solution) AND D9030SATC (current solution nomenclature) prompt. If not, the products did not properly handle BIST Activate FIS; a non-standard way to make it produce the desired pattern will be required.

Test Procedure:

This parameter is covered by Keysight Technologies, Inc. N5411B (legacy solution) AND D9030SATC (current solution nomenclature) automated SATA compliance software, revision 1.65 or later. Either "PASS" or "FAIL" is shown for the 6Gb/s Transmitter Maximum Amplitude test in the report generated at the completion of the testing.

Observable Results:

The 6Gb/s transmitter differential amplitude shall be less than or equal to 900mVpp.

Possible Problems:

Some products may not support disconnect during the process of enabling BIST and testing. For these products, refer to the Disconnect sections of reference [5] for setup requirement.

Test TSG-15 - Gen3 (6.0Gbps) Transmitter Minimum Differential Voltage Amplitude

Purpose: To verify that the Minimum Amplitude of the product's transmitter is within the conformance limits.

References:

[1] Serial ATA Revision 3.0, 7.2.1, Table 31 – Transmitted Signal Requirements
[2] Ibid, 7.2.2.2.7
[3] Ibid, 7.3.2.4, 7.4.3
[4] SATA Interoperability Program Unified Test Document, 2.15.15 – Gen3(6Gb/s) Minimum Differential Voltage Amplitude
[5] Pre-Test MOI

Resource Requirements:

Same as for TSG-01.

See appendix A for details.

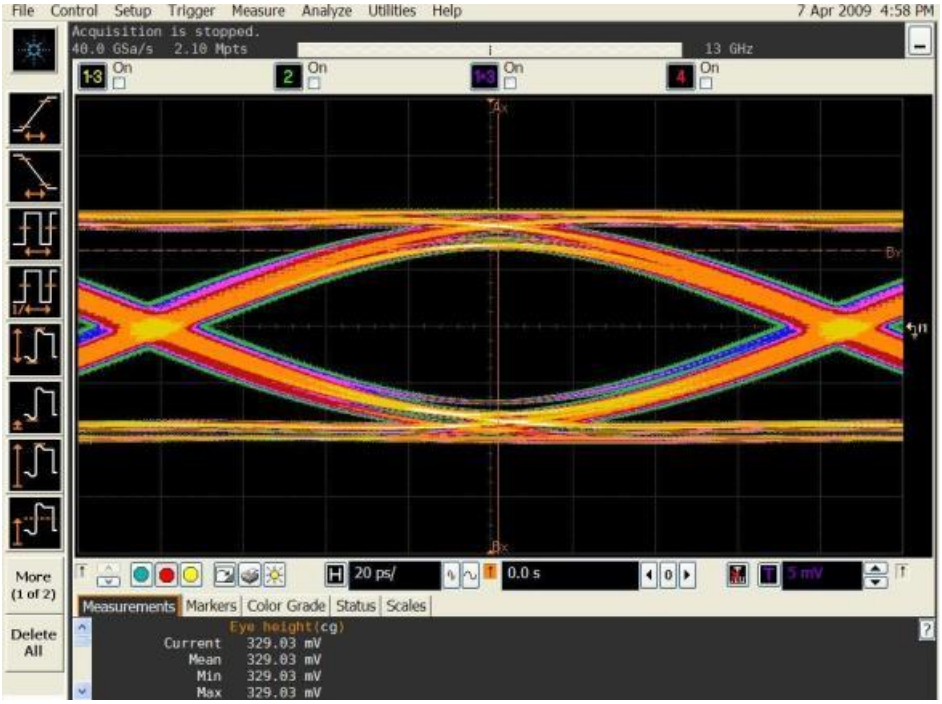
Last Template Modification: May 3, 2013 (Version 1.65)

Discussion:

Reference [1] specifies the Transmitted Signal conformance limits for SATA products. Reference [2] provides the definition of this term for the purposes of SATA testing. Reference [3] defines the measurement requirements for this test.

The minimum TX differential amplitude is a measurement of the minimum eye opening terminated into a laboratory load after the CIC, measured at the 50% location of the bit interval. The amplitude distribution will be measured to include a minimum of 5E+6 Unit Intervals of data. The Lone-Bit Pattern (LBP) is used for this measurement, and the 50% eye location is determined by the compliant, JTF-defined PLL clock recovery defined in [3]. The minimum TX differential amplitude is a measurement of the minimum eye opening, using the specified method, after the Gen3i CIC. For a Gen3u UHost PUT, the Gen3i CIC channel is not used and the measurement is made directly into the lab load.

This test requirement is only applicable to products running at 6Gb/s.



Minimum Voltage Measurement of LBP at JTF-Defined clock location (50%) with 5E6 Unit Intervals of data

Test Setup:

1. The N5411B (legacy solution) AND D9030SATC (current solution nomenclature) SATA compliance software will prompt for LBP when needed. When prompted, follow the procedures in reference [5] to enable those BIST-TAS patterns. Or keep products in BIST-L.

2. Plug the test fixture into the products. The test fixture is connected to channels 1 and 3 of the scope by two 36" SMA cables (Rosenberger or equivalent). OBSERVE the signal on the scope. If it is correct, press OK in the N5411B (legacy solution) AND D9030SATC (current solution nomenclature) prompt. If not, the products did not properly handle BIST Activate FIS; a non-standard way to make it produce the desired pattern will be required.

Test Procedure:

This parameter is covered by Keysight Technologies, Inc. N5411B (legacy solution) AND D9030SATC (current solution nomenclature) automated SATA compliance software, revision 1.65 or later. Either "PASS" or "FAIL" is shown for the 6Gb/s Transmitter Minimum Amplitude test in the report generated at the completion of the testing.

Observable Results:

The 6Gb/s transmitter differential amplitude shall be greater than or equal to 240mVpp for a device, and 200mVpp for a host.

Possible Problems:

Some products may not support disconnect during the process of enabling BIST and testing. For these products, refer to the Disconnect sections of reference [5] for setup requirement.

Test TSG-16 - Gen3 (6.0Gbps) Transmitter AC Common Mode Voltage (Obsolete)

Purpose: To verify that the AC Common Mode Voltage of the product's transmitter is within the conformance limits.

References:

[1] Serial ATA Revision 3.0, 7.2.1, Table 31 – Transmitted Signal Requirements
[2] Ibid, 7.2.2.2.12
[3] Ibid, 7.4.21
[4] SATA Interoperability Program Unified Test Document, 2.15.16 – Gen3(6Gb/s) AC Common Mode Voltage
[5] Pre-Test MOI

Resource Requirements:

Same as for TSG-01.

See appendix A for details.

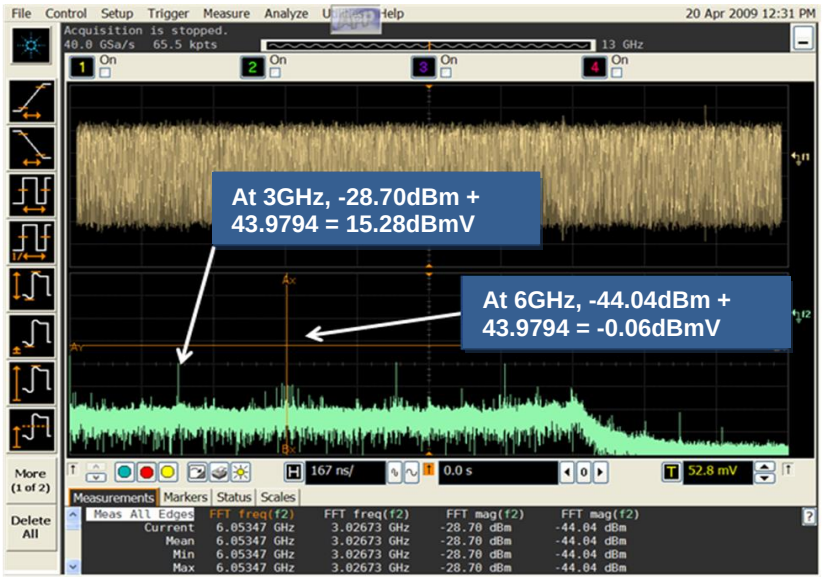
Last Template Modification: May 3, 2013 (Version 1.65)

Discussion:

Reference [1] specifies the Transmitted Signal conformance limits for SATA products. Reference [2] provides the definition of this term for the purposes of SATA testing. Reference [3] defines the measurement requirements for this test.

The common mode signal is created by summing TX+ with TX- and dividing by two. It is imperative to have completely deskewed the measurement inputs of the laboratory load out to the compliance point to minimize any common mode components due to phase misalignment. AC common mode voltage is measured in the frequency domain, using a Gaussian windowing method, similar to a spectrum analyzer. Resolution bandwidth for this measurement is set to 1MHz. The span for the measurement of the fundamental frequency at 3GHz is from -5350ppm to +350ppm relative to 3GHz. The span for the measurement of the 2nd harmonic at 6GHz is from -5350ppm to +350ppm, relative to 6GHz.

This test requirement is only applicable to products running at 6Gb/s.



Frequency domain measurement of 3GHz and 6GHz common mode voltage magnitude

Test Setup:

1. The N5411B (legacy solution) AND D9030SATC (current solution nomenclature) SATA compliance software will prompt for HFTP when needed. When prompted, follow the procedures in reference [5] to enable those BIST-TAS patterns. Or keep products in BIST-L.

2. Plug the test fixture into the products. The test fixture is connected to channels 1 and 3 of the scope by two 36" SMA cables (Rosenberger or equivalent). OBSERVE the signal on the scope. If it is correct, press OK in the N5411B (legacy solution) AND D9030SATC (current solution nomenclature) prompt. If not, the products did not properly handle BIST Activate FIS; a non-standard way to make it produce the desired pattern will be required.

Test Procedure:

This parameter is covered by Keysight Technologies, Inc. N5411B (legacy solution) AND D9030SATC (current solution nomenclature) automated SATA compliance software, revision 1.65 or later. Either "PASS" or "FAIL" is shown for the 6Gb/s Transmitter AC Common Mode Voltage test in the report generated at the completion of the testing.

Observable Results:

The Transmitter shall not deliver more output voltage than the following limits:

- Fundamental (3 GHz): Max = 26 dBmV(pk)
- 2nd Harmonic (6 GHz): Max = 30 dBmV(pk)

Possible Problems:

Some products may not support disconnect during the process of enabling BIST and testing. For these products, refer to the Disconnect sections of reference [5] for setup requirement.

Test TSG-17 – Gen3 (6.0Gbps) Transmitter Emphasis

Purpose: To verify that the Transmitter Emphasis of the product's transmitter is within the conformance limits.

References:

[1] Serial ATA Revision 3.4, 7.6.33, Table 54 – Transmitted Signal Requirements
[2] Ibid, 7.4.3.3.14
[3] Ibid, 7.6.33
[4] SATA Interoperability Program Unified Test Document Revision 1.6 2.7.19 – Gen3(6Gb/s) Tx Emphasis
[5] Pre-Test MOI

Resource Requirements:

Same as for TSG-01.

See appendix A for details.

Discussion:

Reference [1] specifies the Transmitted Signal conformance limits for SATA products. Reference [2] provides the definition of this term for the purposes of SATA testing. Reference [4] defines the measurement requirements for this test.
Reference [3] outlines two methods for evaluating Transmitted Signal emphasis levels. TSG-17 requires passing at least one of the Device TX Emphasis test methods to achieve specification compliance for Device Tx Emphasis.
The SATA automation system N5411B (legacy solution) AND D9030SATC (current solution nomenclature) currently does not implement the alternate Peak-Mode (TP#83) methodology described in Reference [2].

Test Setup:

1. The N5411B (legacy solution) AND D9030SATC (current solution nomenclature) SATA compliance software will prompt for MFTP when needed. When prompted, follow the procedures in reference [5] to enable those BIST-TAS patterns. Or keep products in BIST-L.

2. Plug the test fixture into the products. The test fixture is connected to channels 1 and 3 of the scope by two 36" SMA cables (Rosenberger or equivalent). OBSERVE the signal on the scope. If it is correct, press OK in the N5411B (legacy solution) AND D9030SATC (current solution nomenclature) prompt. If not, the products did not properly handle BIST Activate FIS; a non-standard way to make it produce the desired pattern will be required.

Test Procedure (A):

This parameter is covered by Keysight Technologies, Inc. N5411B (legacy solution) AND D9030SATC (current solution nomenclature) automated SATA compliance software, revision 1.82 or later. Either "PASS" or "FAIL" is shown for the 6Gb/s Transmitter AC Common Mode Voltage test in the report generated at the completion of the testing.

Observable Results:

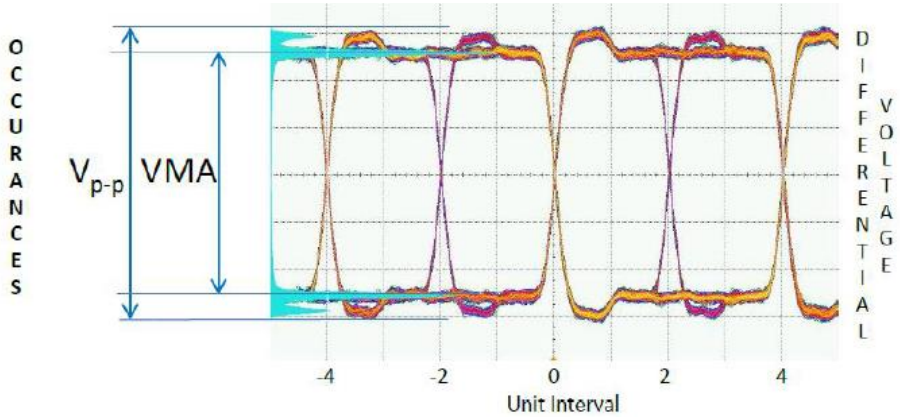
The Transmitter emphasis shall be within the limits shown in the table below

Parameter	Limit	Gen3i Emphasis (dB)	Gen3u Emphasis (dB)
$V_{EmphasisDevice}$ Device Tx Emphasis	Min	0.5	-
	Max	2.5	-
$V_{EmphasisHost}$ Host Tx Emphasis	Min	-2	-2
	Max	1.5	1.5

This parameter is covered by Keysight Technologies, Inc. N5411B (legacy solution) AND D9030SATC (current solution nomenclature) automated SATA compliance software,

Test Procedure (B): Emphasis Peak Mode Method (TP #83)

An alternate emphasis methodology introduced in TP #83 leverages a peak mode approach.



SATA 3.4: Figure 252 - Transmitter Emphasis Measurement (Alternate Method)

The following formula shall be used to calculate the transmitter equalization value:

Transmitter equalization = 20 × log(VP-P / VMA) dB

where:

VP-P is the peak to peak value; and

VMA is the mode value.

Observable Results (B):

The Transmitter emphasis shall be within the limits shown in the table below

Parameter	Limit	Gen3i Emphasis (dB)
$V_{EmphasisDevice}$, Peak-Mode Device TX Emphasis	Min	0.5
	Max	2.5

This parameter is **not** covered by Keysight Technologies, Inc. N5411B (legacy solution) AND D9030SATC (current solution nomenclature) automated SATA compliance software,

Possible Problems:

Some products may not support disconnect during the process of enabling BIST and testing. For these products, refer to the Disconnect sections of reference [5] for setup requirement.

PHY OOB REQUIREMENTS

Overview:

This group of tests verifies the Phy OOB Requirements, as defined in Section 2.18 of the SATA Interoperability Unified Test Document, v1.6 (which references the Serial ATA Revision 3.4).

Test OOB-01 – OOB Signal Detection Threshold

Purpose: To verify that the OOB Signal Detection Threshold of the Product Under Test's (PUT's) receiver is within the conformance limits.

References:

[1] Serial ATA Revision 3.0, 7.2.1, Table 34 – OOB Specifications
[2] Ibid, 7.2.2.6.2
[3] Ibid, 7.4.24
[4] SATA Interoperability Program Unified Test Document, 2.18.1 – OOB Signal Detection Threshold

Resource Requirements:

- Keysight DSAX93204A, DSAX92804A, DSAX92504A, DSAX92004A and DSAX91604A (32GHz, 28GHz, 25GHz, 20GHz and 16GHz bandwidth, 80GS/s per channel) or Keysight DSA91204A (12GHz bandwidth, 40GS/s per channel)
- Keysight N5411B (legacy solution) AND D9030SATC (current solution nomenclature) SATA 6 Gb/s Compliance Test Software
- Wilder Technologies SATA Gen3 Receptacle Adapter SATA-TPA-R or ICT-Lanto SATA Receptacle Gen 3 TF-1R31 or Crescent Heart Software TF-SATA-NE/ZP or TF-eSATA-NE/ZP test adapter or equivalent
- Keysight N4903B J-BERT (with Option 002) or Keysight 81134A 2-channel 3.35GHz Pulse/Pattern Generator
- Keysight 8493C-020 20dB DC-26.5GHz Passive Attenuator (Qty. 2 needed)
- Keysight 11636B Power Divider (not power splitter) DC-26.5GHz (Qty. 2 needed)
- Keysight 5062-6681 6-inch SMA cable (Qty. 4 needed to mix N4903B or 81134A outputs for OOB testing)

See appendix A for details.

Last Template Modification: March 25, 2009 (Version 1/02)

Discussion:

Reference [1] specifies the Transmitted Signal conformance limits for SATA products. This specification includes conformance limits for the OOB Signal Detection Threshold. Reference [2] provides the definition of this term for the purposes of SATA testing. Reference [3] defines the measurement requirements for this test.

This measurement is performed by having the N4903B or 81134A continuously issue a nominal OOB COMRESET/COMINIT 6 burst sequence and to monitor the products COMINIT and COMWAKE response. This test is run twice to ensure that the product correctly responds to a 210mV amplitude OOB sequence and that the product correctly rejects a 40mV (Gen 1) or 60mV (Gen2 or Gen3) amplitude OOB sequence. When a device detects COMRESET from the host, it should respond with COMINIT. If the device supports asynchronous recovery (ASR), then it may send unsolicited COMINITs. The timing of the COMRESET repetition is then adjusted to ensure an accurate test. When a host detects COMINIT from the device, it should respond with COMWAKE. If the host supports asynchronous recovery, it may respond with COMINIT. Usually the host will respond with COMWAKE properly upon receiving every other COMINIT.

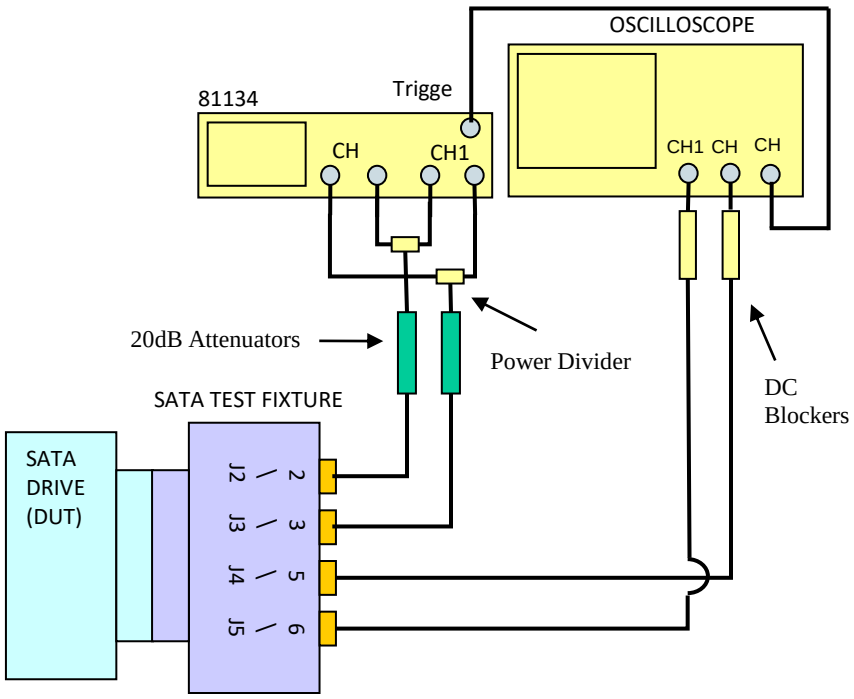
Test Setup:

The following setup diagram, provided in the Keysight N5411B (legacy solution) AND D9030SATC (current solution nomenclature) SATA test software prior to running the OOB tests, will guide the correct connection of the 11636B Power Dividers to the inputs of the Keysight N4903B J-BERT or 81134A Pattern Generator using the 5062-6681 short SMA cables. This allows for the electrical idle to be properly generated by the pattern generator prior to sending the OOB signals to the products. Most pattern generators cannot generate a tri-state signal with proper electrical idle, and power dividers must be used to create these tri-level signals from two channels of a dual-state pattern generator output. More information

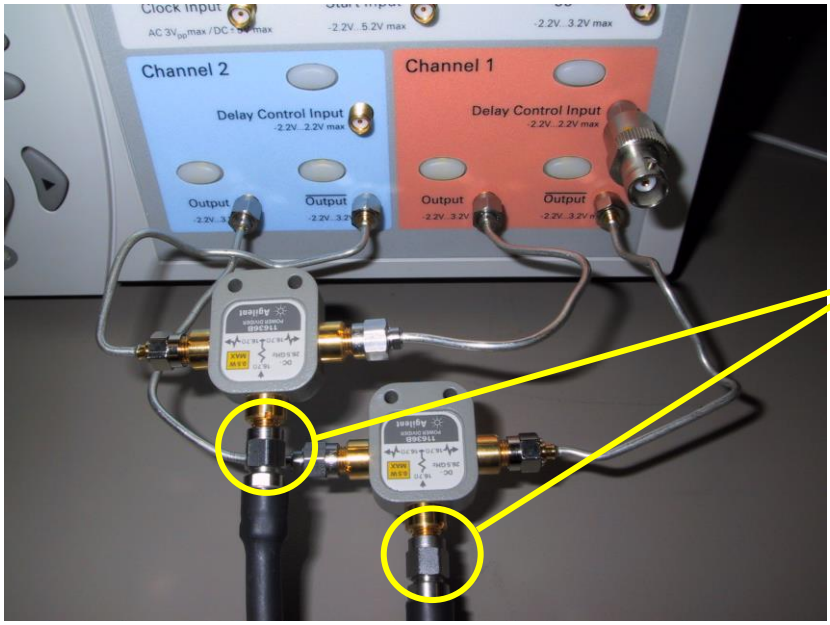
on this setup procedure can be found in Annex A. In order to maintain the proper differential polarity and pattern disparity, it is important to ensure that the Channel 1 positive (+) output of the 81134A is mixed with the Channel 2 negative (-) output of the 81134A, as shown in the following diagram, to provide the TX+ signal that will be delivered to the RX+ input on the products. The remaining 81134A data outputs, Channel 1 negative (-) and Channel 2 positive (+) are mixed together and delivered to the RX- input on the products through the Crescent Heart Software TF-SATA-NE/ZP or TF-eSATA-NE/ZP test adapter or equivalent. As for the N4903B J-BERT, the Data Out (+) is mixed with Aux Data Out (+) to obtain TX+ signal while the Data Out (-) is mixed with Aux Data Out (-) to obtain TX- signal.

The OOB Tests are designed to be run concurrently for simplicity. Since the initiation of a COMRESET from a products or pattern generator will force a hard reset in a products, the following OOB tests can all be performed using an Keysight N4903B J-BERT or 81134A 3.35Gbps Programmable Pulse/Pattern Generator to generate the nominal OOB COMRESET and COMWAKE bursts, as well as to stress the minimum and maximum voltage threshold conditions for OOB Signal Detections. The Keysight Infiniium oscilloscope, which is running the N5411B (legacy solution) AND D9030SATC (current solution nomenclature) SATA test software, will control the pattern generator stimulus as well as the oscilloscope acquisition and processing parameters, providing fully automated control and repeatability of the OOB test sequence in successive fashion. A COMRESET is issued from the generator prior to running each test to ensure products reset, but in some cases, it may still be necessary to remove power from the products under test temporarily to allow the products to exit from a BIST controlled mode and return to normal operation.

Example OOB Setup for a SATA Device:



The N5411B (legacy solution) AND D9030SATC (current solution nomenclature) software includes a calibration routine to verify the amplitudes for the OOB bursts used to test OOB minimum threshold detection amplitude at 40mV and 210mV for Gen1 products and 60mV and 210mV for Gen2 or Gen3 products.



When the 40mV of differential OOB amplitude is needed at the products receiver, then insert the 8493C-020 20dB passive attenuators here, one on each of the 11636B power divider outputs, before the SMA cable is attached. The voltage output of the 81134A after the attenuator is now 10 times lower than the voltage selection on the 81134A output. The sensitivity of the adjustment is now 0.1mV instead of 1mV with the "divide-by-10" attenuator in place.

Test Procedure:

This parameter is covered by Keysight Technologies, Inc. N5411B (legacy solution) AND D9030SATC (current solution nomenclature) automated SATA compliance software, revision 1.65 or later. Either "PASS" or "FAIL" is shown for the OOB Signal Detection Threshold test in the report generated at the completion of the testing.

To execute this test on a products which supports ONLY 1.5Gb/s, an OOB burst is issued to the products at the following voltage threshold limits:

- 40mV (at this limit, the products is expected to **NOT DETECT** the OOB signaling)
- 210mV (at this limit, the products is expected to **DETECT** the OOB signaling)

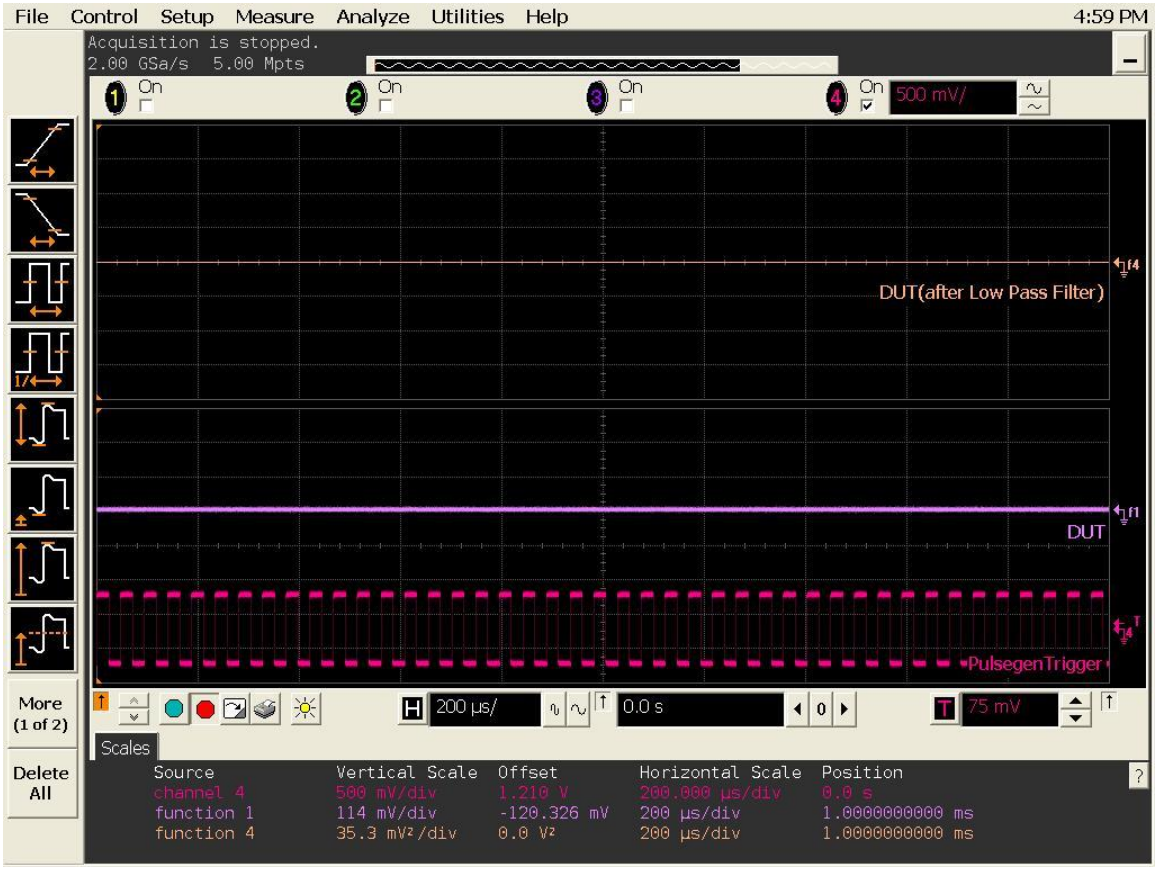
To execute this test on a products which supports 3Gb/s or 6Gb/s, an OOB burst is issued to the products at the following voltage threshold limits:

- 60mV (at this limit, the products is expected to **NOT DETECT** the OOB signaling)
- 210mV (at this limit, the products is expected to **DETECT** the OOB signaling)

Example Typical products behavior for in specification COMINIT/COMRESET sequence at 210mV

In this figure, the product correctly responds to a valid in-spec COMRESET/COMWAKE OOB initialization sequence at 210mV, thus passing the threshold test. The other requirement for passing is to successfully REJECT the same HOST OOB signal sent at 40mV (for Gen 1i) or 60mV (for Gen 2i).

Example Typical products behavior for out of specification COMINIT/COMRESET sequence at 40mV or 60mV



Observable Results:

Verify that the products consistently response to each COMINIT/COMRESET sequence under the following sequence parameters:

6 x (COMINIT/COMRESET burst + 480UI gap)
+1 x (45,000UI gap)

Verify that the products respond consistently to each COMINIT sequence when voltage threshold is changed to 210mV

Verify that the products does not respond consistently when voltage threshold is changed to 40mV (Gen1 only) or 60mV (Gen 2 or Gen3)

Pass/Fail Criteria

- For products running at 1.5Gb/s ONLY:
  - Verification of **NO** products OOB detection at 40mV
  - Verification of products OOB detection at 210mV
  - If any of the above cases fails, this is considered a failure by the products.
- For products running at 3Gb/s or 6Gb/s:
  - Verification of **NO** products OOB detection at 60mV
  - Verification of products OOB detection at 210mV
  - If any of the above cases fails, this is considered a failure by the products.

Test OOB-02 – UI During OOB Signaling

Purpose: To verify that the UI During OOB Signaling of the Product Under Test's (PUT's) transmitter is within the conformance limits.

References:

[1] Serial ATA Revision 3.0, 7.2.1, Table 34 – OOB Specifications
[2] Ibid, 7.2.2.6.3
[3] Ibid, 7.4.14
[4] SATA Interoperability Program Unified Test Document, 2.18.2 – UI During OOB Signaling

Resource Requirements:

- Keysight DSAX93204A, DSAX92804A, DSAX92504A, DSAX92004A and DSAX91604A (32GHz, 28GHz, 25GHz, 20GHz and 16GHz bandwidth, 80GS/s per channel) or Keysight DSA91204A (12GHz bandwidth, 40GS/s per channel)
- Keysight N5411B (legacy solution) AND D9030SATC (current solution nomenclature) SATA 6 Gb/s Compliance Test Software
- Wilder Technologies SATA Gen3 Receptacle Adapter SATA-TPA-R or ICT-Lanto SATA Receptacle Gen 3 TF-1R31 or Crescent Heart Software TF-SATA-NE/ZP or TF-eSATA-NE/ZP test adapter or equivalent
- Keysight N4903B (with Option 002) or Keysight 81134A 2-channel 3.35GHz Pulse/Pattern Generator
- Keysight 11636B Power Divider (not power splitter) DC-26.5GHz (Qty. 2 needed)
- Keysight 5062-6681 6-inch SMA cable (Qty. 4 needed to mix N4903B or 81134A outputs for OOB testing)

See Appendix A for details.

Last Template Modification: May 3, 2013 (Version 1.65)

Discussion:

Reference [1] specifies the Transmitted Signal conformance limits for SATA products. This specification includes conformance limits for the UI During OOB Signaling. Reference [2] provides the definition of this term for the purposes of SATA testing. Reference [3] defines the measurement requirements for this test.

Test Setup:

The OOB Tests are designed to be run concurrently for simplicity. Since the initiation of a COMRESET from a products or pattern generator will force a hard reset in a products, the following OOB tests can all be performed using an Keysight N4903B J-BERT or 81134A 3.35Gbps Programmable Pulse/Pattern Generator to generate the nominal OOB COMRESET and COMWAKE bursts, as well as to stress the min in-spec, max in-spec, min out-of-spec and max out-of-spec timing conditions for inter-burst gaps. The Keysight oscilloscope, which is running the N5411B (legacy solution) AND D9030SATC (current solution nomenclature) SATA test software, will control both the pattern generator stimulus as well as the oscilloscope acquisition and processing parameters, providing fully automated control and repeatability of the OOB test sequence in successive fashion. A COMRESET is issued from the generator prior to running each test to ensure products reset, but in some cases, it may still be necessary to remove power from the products under test temporarily to allow the products to exit from a BIST controlled mode and return to normal operation.

Test Procedure:

This parameter is covered by Keysight Technologies, Inc. N5411B (legacy solution) AND D9030SATC (current solution nomenclature) automated SATA compliance software, revision 1.65 or later. Either "PASS" or "FAIL" is shown for the UI During OOB Signaling test in the report generated at the completion of the testing.

Observable Results:

The Mean UI During OOB Signaling value shall be between 646.67 and 686.67ps.

Possible Problems:

Test OOB-03 – COMINIT/RESET and COMWAKE Transmit Burst Length

Purpose: To verify that the COMINIT/RESET and COMWAKE Transmit Burst Length of the Product Under Test's (PUT's) transmitter is within the conformance limits.

References:

[1] Serial ATA Revision 3.0, 7.2.1, Table 34 – OOB Specifications
[2] Ibid, 7.2.2.6.4
[3] Ibid, 7.4.2251
[4] SATA Interoperability Program Unified Test Document, 2.18.3 – COMINIT/RESET and COMWAKE Transmit Burst Length

Resource Requirements:

Same as for OOB-02.

See appendix A for details.

Last Template Modification: May 3, 2013 (Version 1.65)

Discussion:

Reference [1] specifies the Transmitted Signal conformance limits for SATA products. This specification includes conformance limits for the COMINIT/RESET and COMWAKE Transmit Burst Length. Reference [2] provides the definition of this term for the purposes of SATA testing. Reference [3] defines the measurement requirements for this test.

Test Setup:

The OOB Tests are designed to be run concurrently for simplicity. Since the initiation of a COMRESET from a products or pattern generator will force a hard reset in a products, the following OOB tests can all be performed using an Keysight N4903B J-BERT or 81134A 3.35Gbps Programmable Pulse/Pattern Generator to generate the nominal OOB COMRESET and COMWAKE bursts, as well as to stress the min in-spec, max in-spec, min out-of-spec and max out-of-spec timing conditions for inter-burst gaps. The Keysight oscilloscope, which is running the N5411B (legacy solution) AND D9030SATC (current solution nomenclature) SATA test software, will control both the pattern generator stimulus as well as the oscilloscope acquisition and processing parameters, providing fully automated control and repeatability of the OOB test sequence in successive fashion. A COMRESET is issued from the generator prior to running each test to ensure products reset, but in some cases, it may still be necessary to remove power from the products under test temporarily to allow the products to exit from a BIST controlled mode and return to normal operation.

Test Procedure:

This parameter is covered by Keysight Technologies, Inc. N5411B (legacy solution) AND D9030SATC (current solution nomenclature) automated SATA compliance software, revision 1.65 or later. Either "PASS" or "FAIL" is shown for the products COMINIT and COMWAKE Transmit Burst Length test in the report generated at the completion of the testing.

Observable Results:

The products COMINIT and COMWAKE Transmit Burst Length value shall be between the minimum and maximum values of UI_{OOB} multiplied by 160. Numerically, the COMINIT and COMWAKE burst lengths should be between 103.5 ns and 109.9 ns, which is 160 times the Min and Max UI_{OOB} specification limits of 646.67ps and 686.67ps, respectively. Note that this measurement is made as the longest burst length between the +100mV threshold crossing and -100mV threshold crossing within each COMRESET/COMINIT/COMWAKE burst.

Possible Problems:

If this measurement is only made at the +100mV or -100mV threshold, some bits in the OOB burst will not be measured correctly and may result in a measurement failure.

Test OOB-04 – COMINIT/RESET Transmit Gap Length

Purpose: To verify that the COMINIT/RESET Transmit Gap Length of the Product Under Test's (PUT's) transmitter is within the conformance limits.

References:

[1] Serial ATA Revision 3.0, 7.2.1, Table 34 – OOB Specifications
[2] Ibid, 7.2.2.6.5
[3] Ibid, 7.4.25
[4] SATA Interoperability Program Unified Test Document, 2.17.4 – COMINIT/RESET Transmit Gap Length

Resource Requirements:

Same as for OOB-02.

Last Template Modification: May 3, 2013 (Version 1.65)

Discussion:

Reference [1] specifies the Transmitted Signal conformance limits for SATA products. This specification includes conformance limits for the COMINIT/RESET Transmit Gap Length. Reference [2] provides the definition of this term for the purposes of SATA testing. Reference [3] defines the measurement requirements for this test.

Test Setup:

The OOB Tests are designed to be run concurrently for simplicity. Since the initiation of a COMRESET from a products or pattern generator will force a hard reset in a products, the following OOB tests can all be performed using an Keysight N4903B J-BERT or 81134A 3.35Gbps Programmable Pulse/Pattern Generator to generate the nominal OOB COMRESET and COMWAKE bursts, as well as to stress the min in-spec, max in-spec, min out-of-spec and max out-of-spec timing conditions for inter-burst gaps. The Keysight oscilloscope, which is running the N5411B (legacy solution) AND D9030SATC (current solution nomenclature) SATA test software, will control both the pattern generator stimulus as well as the oscilloscope acquisition and processing parameters, providing fully automated control and repeatability of the OOB test sequence in successive fashion. A COMRESET is issued from the generator prior to running each test to ensure products reset, but in some cases, it may still be necessary to remove power from the products under test temporarily to allow the products to exit from a BIST controlled mode and return to normal operation.

Test Procedure:

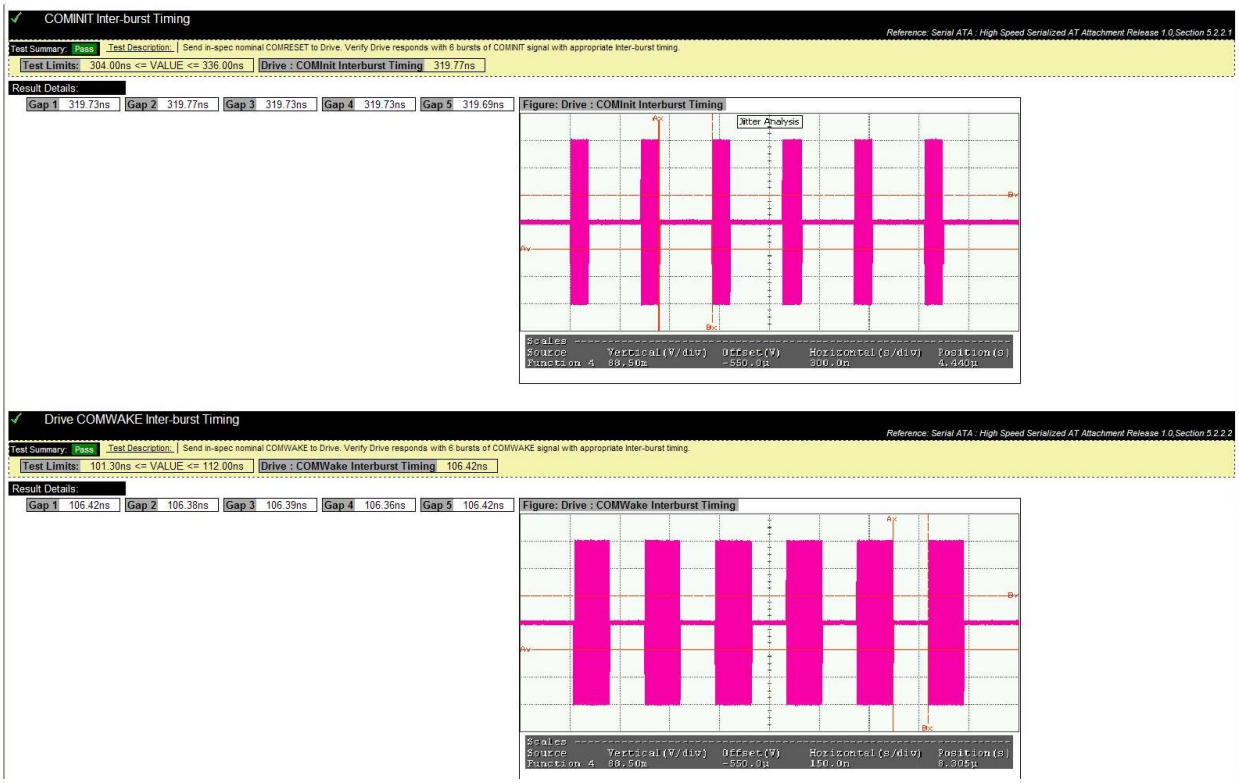
This parameter is covered by Keysight Technologies, Inc. N5411B (legacy solution) AND D9030SATC (current solution nomenclature) automated SATA compliance software, revision 1.65 or later. Either "PASS" or "FAIL" is shown for the products COMINIT/RESET Transmit Gap Length test in the report generated at the completion of the testing.

Observable Results:

The COMINIT/RESET Transmit Gap Length value shall be between the minimum and maximum values of UI_{OOB} multiplied by 480. Numerically, the COMINIT and COMRESET gap lengths should be between 310.4 ns and 329.6 ns, which is 480 times the Min and Max UI_{OOB} specification limits of 646.67ps and 686.67ps, respectively. Note that this measurement is made as the longest burst length between the +100mV threshold crossing and -100mV threshold crossing within each COMRESET/COMINIT/COMWAKE burst.

Possible Problems:

If this measurement is only made at the +100mV or -100mV threshold, some bits in the OOB burst will not be measured correctly and may result in a measurement failure.



Example N5411B (legacy solution) AND D9030SATC (current solution nomenclature) OOB Output Report: This is a section of the HTML output report that illustrates and quantifies the COMINIT and COMWAKE Transmit Gap Lengths.

Test OOB-05 – COMWAKE Transmit Gap Length

Purpose: To verify that the COMWAKE Transmit Gap Length of the Product Under Test's (PUT's) transmitter is within the conformance limits.

References:

[1] Serial ATA Revision 3.0, 7.2.1, Table 34 – OOB Specifications
[2] Ibid, 7.2.2.6.6
[3] Ibid, 7.4.25
[4] SATA Interoperability Program Unified Test Document, 2.18.5 – COMWAKE Transmit Gap Length

Resource Requirements:

Same as for OOB-02.

Last Template Modification: May 3, 2013 (Version 1.65)

Discussion:

Reference [1] specifies the Transmitted Signal conformance limits for SATA products. This specification includes conformance limits for the COMWAKE Transmit Gap Length. Reference [2] provides the definition of this term for the purposes of SATA testing. Reference [3] defines the measurement requirements for this test.

Test Setup:

The OOB Tests are designed to be run concurrently for simplicity. Since the initiation of a COMRESET from a products or pattern generator will force a hard reset in a products, the following OOB tests can all be performed using an Keysight N4903B J-BERT or 81134A 3.35Gbps Programmable Pulse/Pattern Generator to generate the nominal OOB COMRESET and COMWAKE bursts, as well as to stress the min in-spec, max in-spec, min out-of-spec and max out-of-spec timing conditions for inter-burst gaps. The Keysight oscilloscope, which is running the N5411B (legacy solution) AND D9030SATC (current solution nomenclature) SATA test software, will control both the pattern generator stimulus as well as the oscilloscope acquisition and processing parameters, providing fully automated control and repeatability of the OOB test sequence in successive fashion. A COMRESET is issued from the generator prior to running each test to ensure products reset, but in some cases, it may still be necessary to remove power from the products under test temporarily to allow the products to exit from a BIST controlled mode and return to normal operation.

Test Procedure:

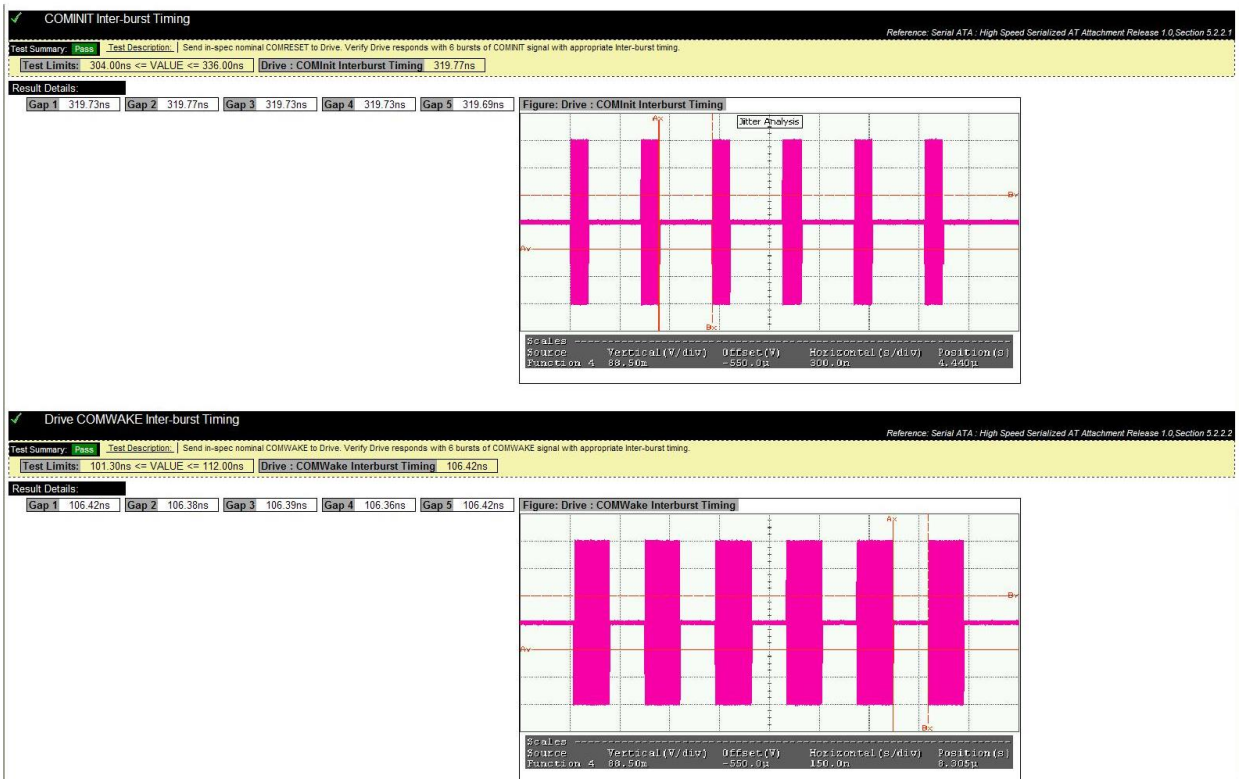
This parameter is covered by Keysight Technologies, Inc. N5411B (legacy solution) AND D9030SATC (current solution nomenclature) automated SATA compliance software, revision 1.65 or later. Either "PASS" or "FAIL" is shown for the products COMWAKE Transmit Gap Length test in the report generated at the completion of the testing.

Observable Results:

The COMWAKE Transmit Gap Length value shall be between the minimum and maximum values of UI_{OOB} multiplied by 160. Numerically, the COMWAKE gap lengths should be between 103.5 ns and 109.9 ns, which is 160 times the Min and Max UI_{OOB} specification limits of 646.67ps and 686.67ps, respectively. Note that this measurement is made as the longest burst length between the +100mV threshold crossing and -100mV threshold crossing within each COMRESET/COMINIT/COMWAKE burst.

Possible Problems:

If this measurement is only made at the +100mV or -100mV threshold, some bits in the OOB burst will not be measured correctly and may result in a measurement failure.



Example N5411B (legacy solution) AND D9030SATC (current solution nomenclature) OOB Output Report: This is a section of the HTML output report that illustrates and quantifies the COMINIT and COMWAKE Transmit Gap Lengths.

Test OOB-06 – COMWAKE Gap Detection Windows

Purpose: To verify that the COMWAKE Gap Detection Windows of the Product Under Test's (PUT's) receiver are within the conformance limits.

References:

[1] Serial ATA Revision 3.0, 7.2.1, Table 34 – OOB Specifications
[2] Ibid, 7.2.2.6.7
[3] Ibid, 7.4.25
[4] SATA Interoperability Program Unified Test Document, 2.18.6 –COMWAKE Gap Detection Windows

Resource Requirements:

Same as for OOB-02.

See Appendix A for details.

Last Template Modification: May 3, 2013 (Version 1.65)

Discussion:

Reference [1] specifies the Transmitted Signal conformance limits for SATA products. This specification includes conformance limits for the COMWAKE Gap Detection Windows. Reference [2] provides the definition of this term for the purposes of SATA testing. Reference [3] defines the measurement requirements for this test.

Complications with Hosts supporting Asynchronous Recovery (ASR): The OOB gap window is currently static in timing and the gap detect window can fail on Hosts supporting ASR. As an interim solution to this static timing problem it recommended to deselect the ASR option in OOB6 and to perform this measurement manually. This is done by using an oscilloscope and manually placing cursors between, the second gap in the COM-Wake/COM-Init (at a -100mv

Test Setup:

The OOB Tests are designed to be run concurrently for simplicity. Since the initiation of a COMRESET from a products or pattern generator will force a hard reset in a products, the following OOB tests can all be performed using an Keysight N4903B J-BERT, M8020A J-Bert or 81134A 3.35Gbps Programmable Pulse/Pattern Generator to generate the nominal OOB COMRESET and COMWAKE bursts, as well as to stress the min in-spec, max in-spec, min out-of-spec and max out-of-spec timing conditions for inter-burst gaps. The Keysight oscilloscope, which is running the N5411B (legacy solution) AND D9030SATC (current solution nomenclature) SATA test software, will control both the pattern generator stimulus as well as the oscilloscope acquisition and processing parameters, providing fully automated control and repeatability of the OOB test sequence in successive fashion. A COMRESET is issued from the generator prior to running each test to ensure products reset, but in some cases, it may still be necessary to remove power from the products under test temporarily to allow the products to exit from a BIST controlled mode and return to normal operation.

Test Procedure:

This parameter is covered by Keysight Technologies, Inc. N5411B (legacy solution) AND D9030SATC (current solution nomenclature) automated SATA compliance software, revision 1.65 or later. Either "PASS" or "FAIL" is shown for the products COMWAKE Gap Detection Windows test in the report generated at the completion of the testing.

Observable Results:

Verify that the products consistently response to each COMINIT/COMWAKE sequence under the following sequence parameters:

For Devices:

6 x (COMINIT/COMRESET burst + 480UI gap) +
1 x (45,000UI gap) +
6 x (COMWAKE burst + 160UI gap) +
1 x (130,000UI gap)

For Hosts:

6 x (COMINIT/COMRESET burst + 480UI gap) +
1 x (300,000UI gap) +
6 x (COMWAKE burst + 160UI gap) +
1 x (130,000UI gap)

Verify that the product continues response to each COMINIT/COMRESET/COMWAKE sequence when COMWAKE gap is changed to 153UI and 167UI.

Verify that the product does not enter speed negotiation when COMWAKE gap is changed to 45UI and 266UI.

Example Typical products behavior for nominal COMINIT/COMRESET and COMWAKE gaps:

Example of products' response to out of specification COMINIT/COMRESET and COMWAKE gaps:

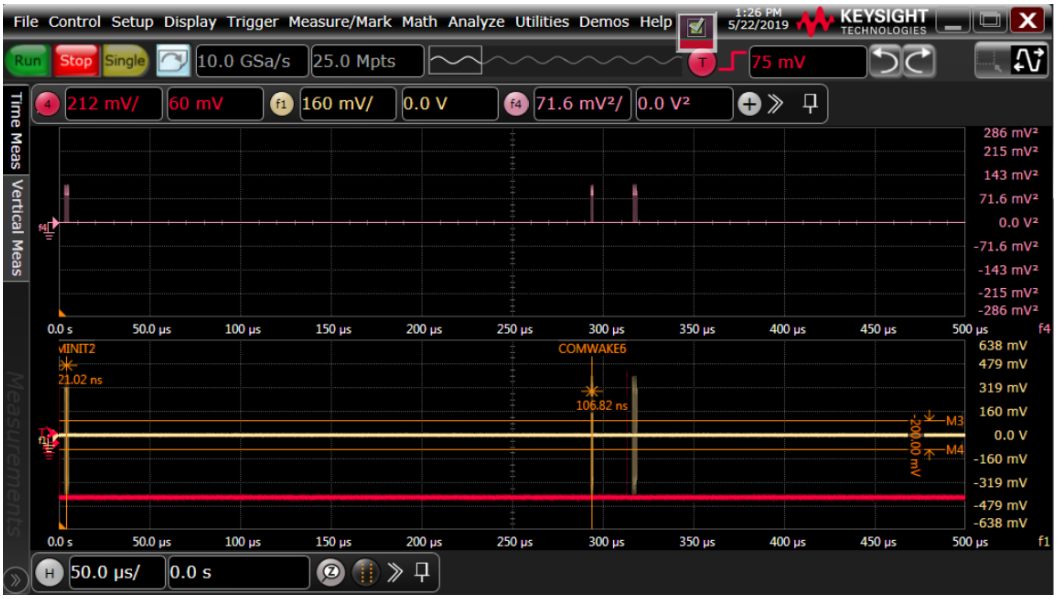
Possible Problems:

NOTE : There is no timing requirement for how soon following a products COMWAKE which the products must respond with a products COMWAKE. For test efficiency purposes, a tester is only required to wait for verification of products COMWAKE up to 100ms following de-qualification of products COMWAKE.

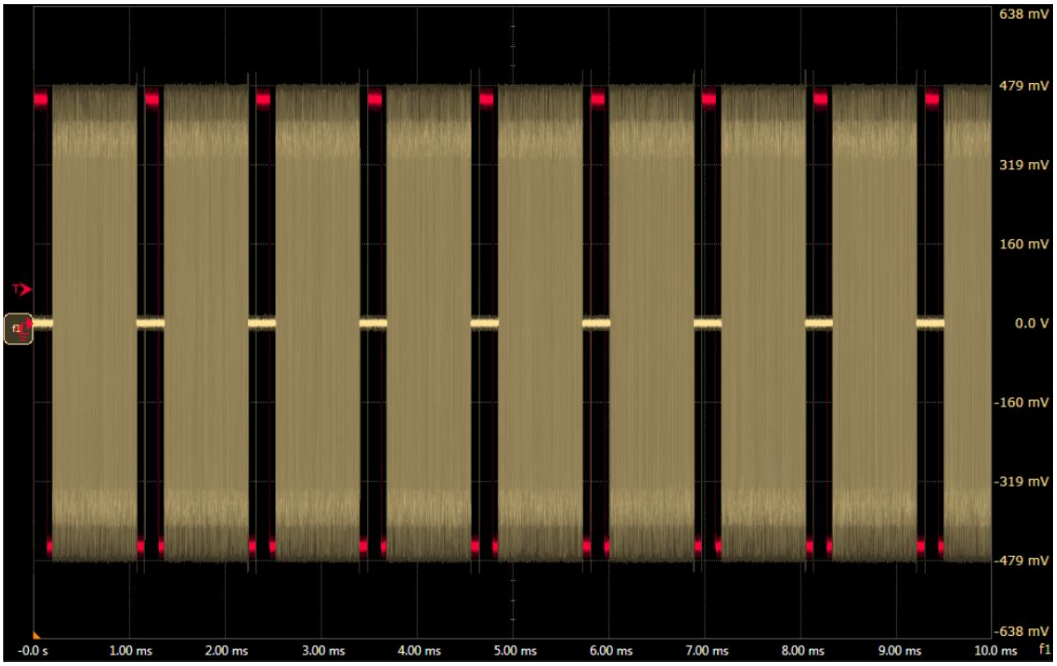
NOTE: Hosts (HUTs) that support ASR can fail OOB-06[a], 06[b] when the COMWAKE response takes longer than the typical non ASR HUT's. Under these conditions the following workaround procedure is recommended until suitable timeout changes can be made in the D9030SATAC test automation tool. The following workaround procedure is advised.

Workaround: Using the Configure Tab on the D9030SATC automation tool, set the OOB Gap and Vthresh Detection Mode to "Manual".

To verify the ASR supported HUT responds with a COMINIT followed by a COMWAKE for OOB-06[a] and 06[b], setup the M8020A and scope to perform a standard OOB-06[a] and 06[b] test and let it complete (this is to setup the instruments). Instruct the M8020A to run manually and capture the COMWAKE response from the HUT as illustrated below. Verify the HUT responds with a COMWAKE as is noted in the screen shot at the 300uS time mark below. This constitutes a passing condition, despite the automated OOB-06[a] and -06[b] failures due to static timing in the D9030SATAC test automation tool.



ASR should be re-enabled, but still operating in “Manual” measurement mode, the test should be repeated to verify that the COMWAKE responds reliably over a 10mS interval. This would constitute a passing condition for OOB-06[a] and -06[b] tests.



Test OOB-07 – COMINIT Gap Detection Windows

Purpose: To verify that the COMINIT Gap Detection Windows of the Product Under Test's (PUT's) receiver are within the conformance limits.

References:

[1] Serial ATA Revision 3.0, 7.2.1, Table 34 – OOB Specifications
[2] Ibid, 7.2.2.6.8
[3] Ibid, 7.4.25
[4] SATA Interoperability Program Unified Test Document, 2.18.7 – COMINIT Gap Detection Windows

Resource Requirements:

Same as for OOB-02.

See Appendix A for details.

Last Template Modification: May 3, 2013 (Version 1.65)

Discussion:

Reference [1] specifies the Transmitted Signal conformance limits for SATA products. This specification includes conformance limits for the COMINIT Gap Detection Windows. Reference [2] provides the definition of this term for the purposes of SATA testing. Reference [3] defines the measurement requirements for this test.

Test Setup:

The OOB Tests are designed to be run concurrently for simplicity. Since the initiation of a COMRESET from a products or pattern generator will force a hard reset in a products, the following OOB tests can all be performed using an Keysight N4903B J-BERT or 81134A 3.35Gbps Programmable Pulse/Pattern Generator to generate the nominal OOB COMRESET and COMWAKE bursts, as well as to stress the min in-spec, max in-spec, min out-of-spec and max out-of-spec timing conditions for inter-burst gaps. The Keysight oscilloscope, which is running the N5411B (legacy solution) AND D9030SATC (current solution nomenclature) SATA test software, will control both the pattern generator stimulus as well as the oscilloscope acquisition and processing parameters, providing fully automated control and repeatability of the OOB test sequence in successive fashion. A COMRESET is issued from the generator prior to running each test to ensure products reset, but in some cases, it may still be necessary to remove power from the products under test temporarily to allow the products to exit from a BIST controlled mode and return to normal operation.

Test Procedure:

This parameter is covered by Keysight Technologies, Inc. N5411B (legacy solution) AND D9030SATC (current solution nomenclature) automated SATA compliance software, revision 1.65 or later. Either "PASS" or "FAIL" is shown for the products COMINIT Gap Detection Windows test in the report generated at the completion of the testing.

Observable Results:

Verify that the products consistently response to each COMINIT/COMWAKE sequence under the following sequence parameters:

For Device:

6 x (COMINIT/COMRESET burst + 480UI gap)
+1 x (45,000UI gap)

For Host:

6 x (COMINIT/COMRESET burst + 480UI gap)
+1 x (300,000UI gap)

Verify that the product continues response to each COMINIT/COMWAKE sequence when COMINIT gap is changed to 459UI and 501UI.

Verify that the product does not enter speed negotiation when COMINIT gap is changed to 259UI and 791UI.

Example Typical products behavior for in specification COMINIT gaps:

Example of products's response to out of specification COMINIT gaps:

Possible Problems:

NOTE: A products must respond by transmitting COMINIT within 10ms of de-qualification of a received COMRESET signal (see section 8.4 of Serial ATA Revision 2.6). With this in mind, a test only needs to wait up to 11ms following de-qualification of COMRESET to ensure that the products is responding. If no COMINIT is received in this timeframe, this is considered a failure by the products to this test.

NOTE: In a case where a products supports Asynchronous Signal Recovery, it is possible that a products may transmit COMINIT pro-actively and not in direct response to a COMRESET. In verification of this test requirement, it is essential that the tester be able to extract any COMINIT response which may be as a result of Asynchronous Signal Recovery, and simply verify COMINIT responses as a result of COMRESET receipt from the products.

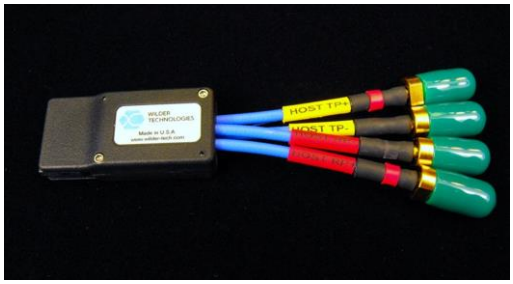
Appendix A – Information on Required Resources

Equipment referred to in this document is described here, or references to available resources are cited.

Information on the Keysight DSAX93204A, DSAX92804A, DSAX92504A, DSAX92004A and DSAX91604A Infiniium 32GHz, 28GHz, 25GHz, 20GHz and 16GHz real time oscilloscopes, and Keysight DSA91204A Infiniium 12GHz real time oscilloscopes and 30GHz InfiniiMax active voltage probes can be found at:
http://www.Keysight.com/find/90000x-series and http://Keysight.com/find/90000a.

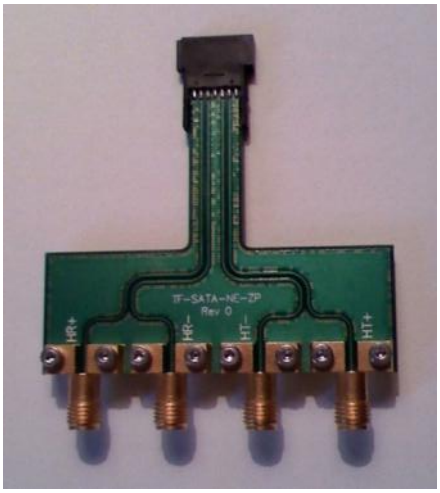
The N5411B (legacy solution) AND D9030SATC (current solution nomenclature) SATA 6 Gb/s Compliance Test Software datasheet and video demonstration can be found at the following URL. The N5411B (legacy solution) AND D9030SATC (current solution nomenclature) datasheet contains a list of necessary test connectors and additional hardware/software products in the 'Ordering Information' section for completing the full set of SATA-IO IW PHY, TSG and OOB tests:
http://www.Keysight.com/find/N5411B (legacy solution) AND D9030SATC (current solution nomenclature)

A picture of the Wilder Technologies SATA Gen3 Receptacle Adapter SATA-TPA-R test fixture or equivalent is shown below for reference. Information about the test fixture can be obtained from their website at:
http://www.wilder-tech.com/sata.htm

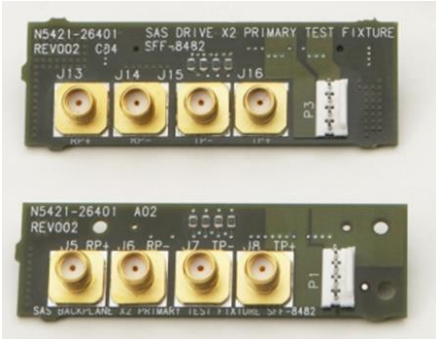


A picture of the ICT-Lanto SATA Receptacle Gen 3 TF-1R31 test fixture or equivalent is shown below for reference. Information about the test fixture can be obtained from their website at:
http://www.ict-lanto.com/product/

A picture of the Crescent Heart Software TF-SATA-NE/ZP or TF-eSATA-NE/ZP test adapter or equivalent is shown below for reference. The TF-SATA-NE/ZP has four SMA(f) connectors labeled appropriately to connect to Host TX+ (HT+), Host TX- (HT-), Host RX+ (HR+) and Host RX- (HR-). Information about the Crescent Heart Software test fixtures can be obtained from their website at:
http://www.c-h-s.com/tf-sata.shtml



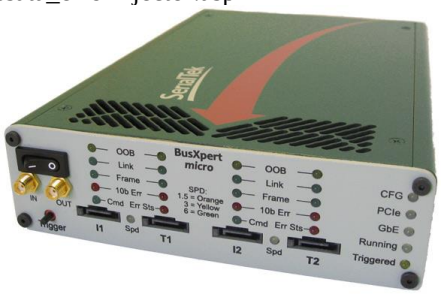
The Keysight Technologies N5421A Receptacle and Plug test fixtures are shown below for reference. The fixtures have four SMA(f) connectors and a power supply connector. Information about Keysight test fixtures can be found at:
www.Keysight.com/find/sata



NOTE: The SATA cable end connector on the fixture is fragile. Support the cables connected to the fixture during connection, testing and disconnect. Do not let their weight be supported by torque on the SATA connector. When unplugging the fixture between tests, grasp the sides of the SATA connector, not the PCB mated to the SATA connector. The easiest way to set up the cables and test fixture for testing is to loosely connect all SMA connectors to the test fixture prior to aligning the SATA connector to the product's SATA connector, then tighten the SMA connections using wrenches once the proper alignment of the SATA connectors is achieved. This will prevent damage to the test connector, and help to ensure a longer life for this sensitive test fixture.

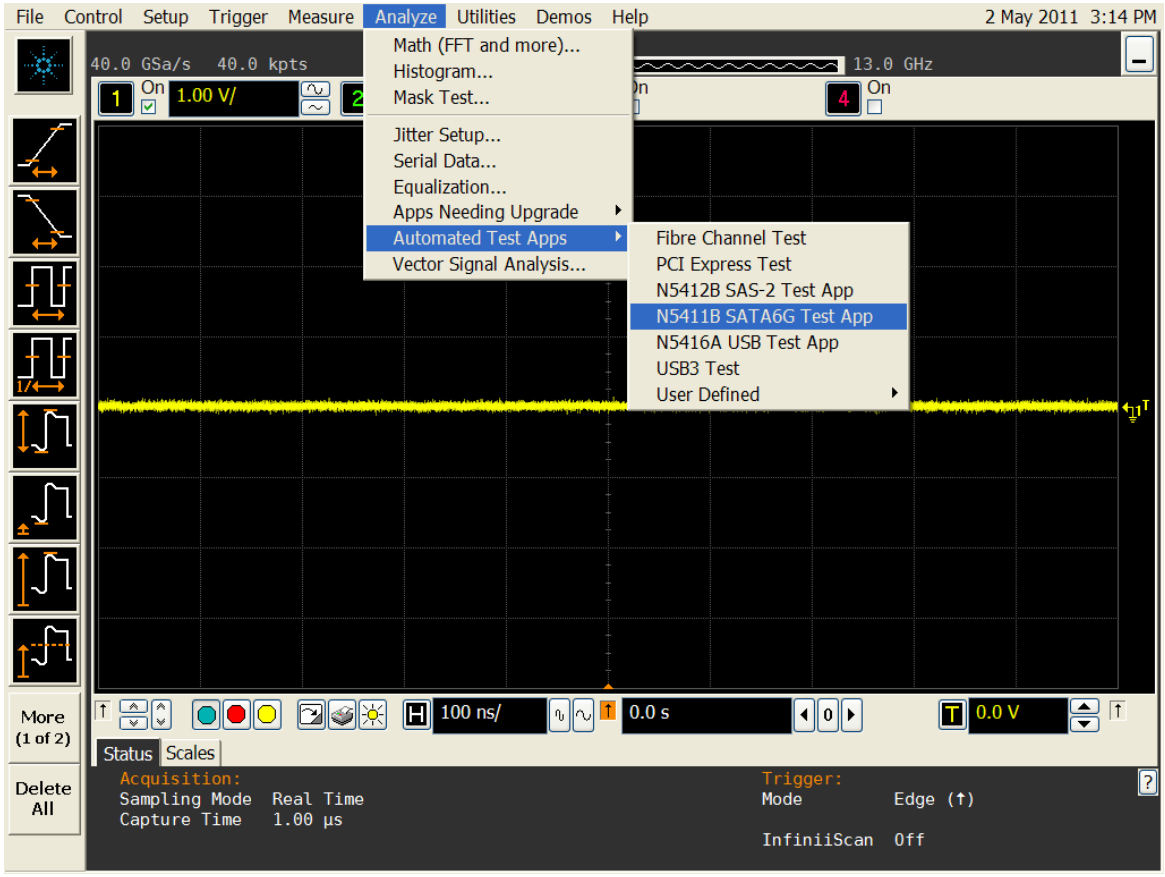
Information about the ULINK Technology, Inc. DriveMaster 2008 and 2010 software can be obtained from their website at:
http://www.ulinktech.com

Information about SerialTek BusMod BusGen BIST Generator as an alternate BIST mode and pattern generation tool can be found from their website at:
http://www.serialtek.com/busmod_sassata_errorinjector.asp

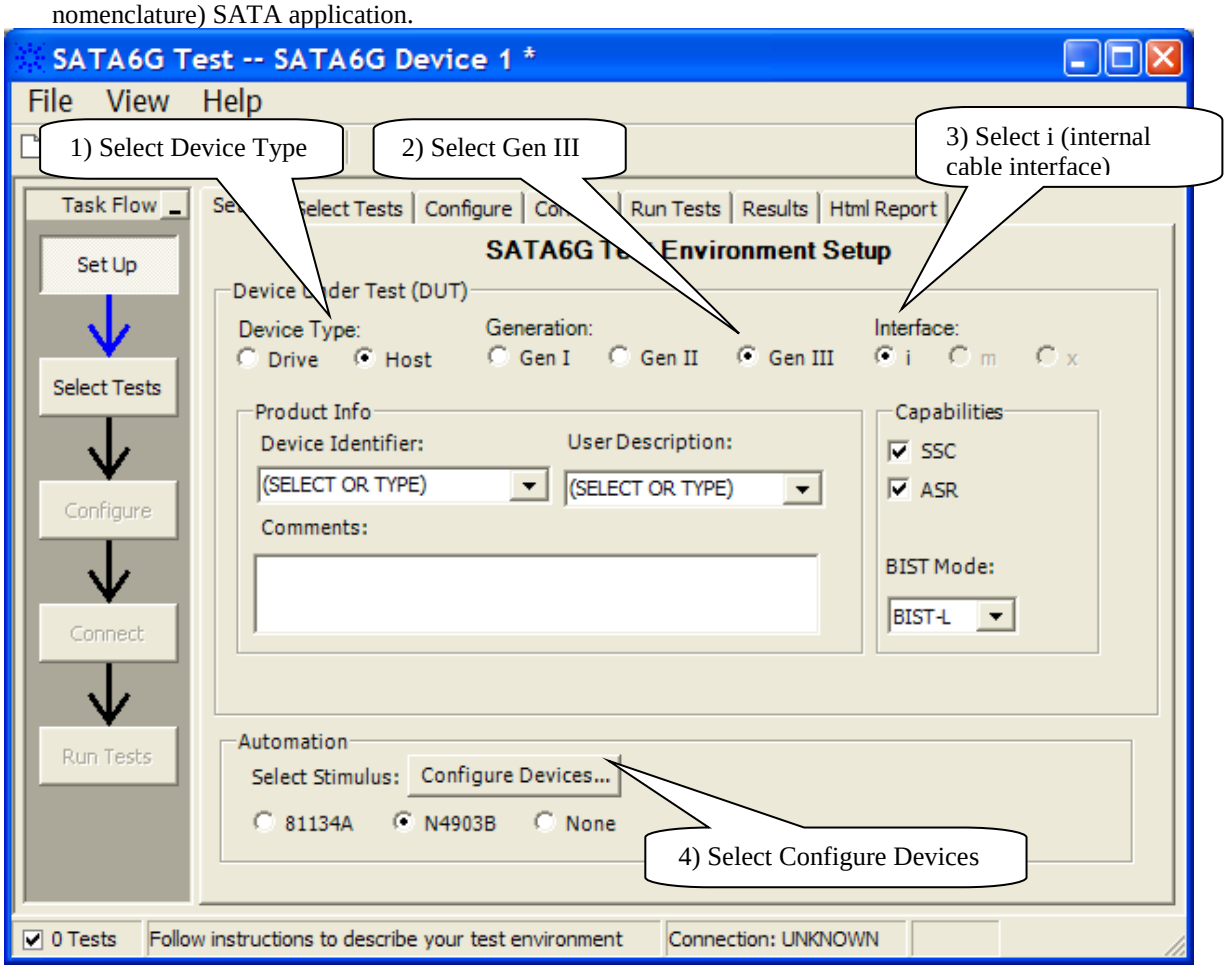


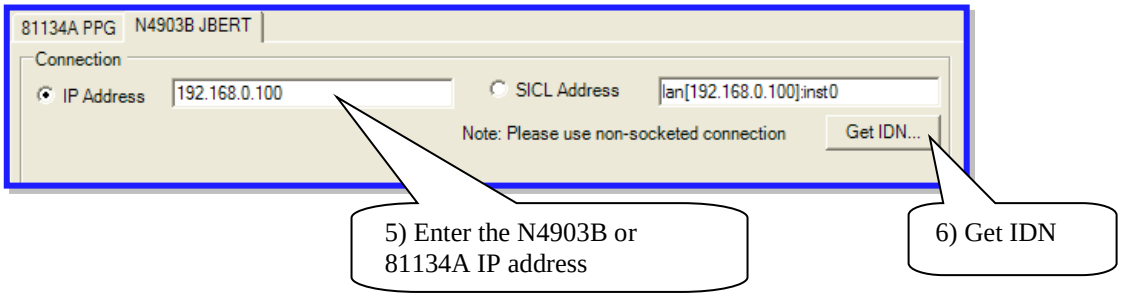
Example N5411B (legacy solution) AND D9030SATC (current solution nomenclature) Product Test Initial Setup Procedure:

1. To start the N5411B (legacy solution) AND D9030SATC (current solution nomenclature) Application, invoke it from the Analyze->Automated Test Apps->SATA menu tree in the Infiniium Oscilloscope interface.

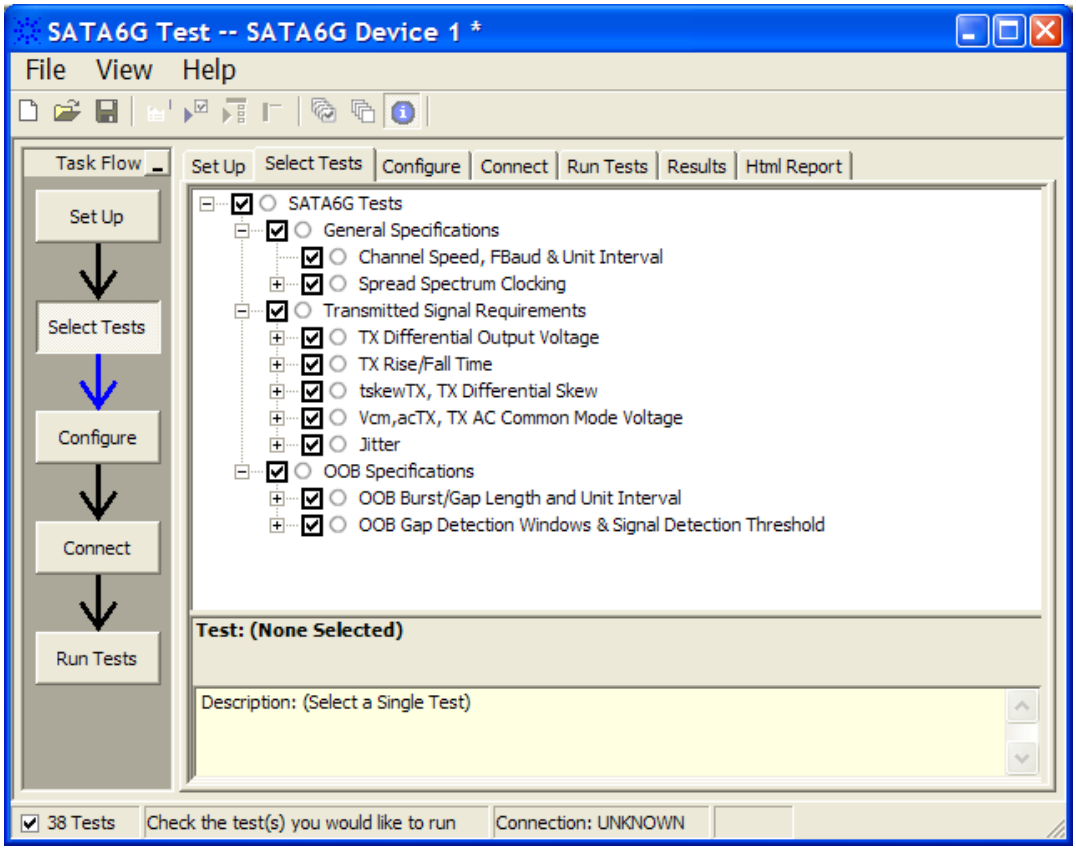


2. Next, choose the type of products that you wish to test and associate the 81134A Programmable Pattern Generator LAN connection with the N5411B (legacy solution) AND D9030SATC (current solution nomenclature) SATA application.

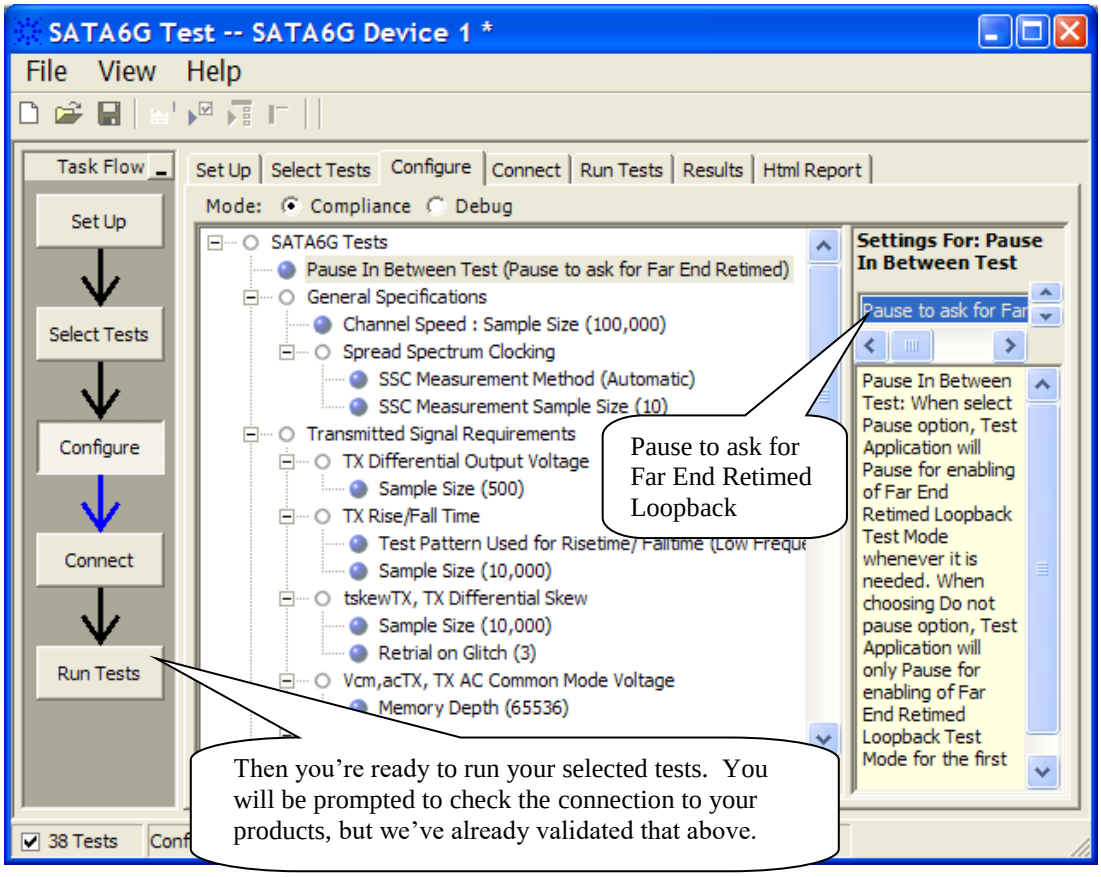




3. Then, click on the "Select Tests" tab and choose the tests that you would like to run. If all tests are desired to be run, then only the top of the main tree needs to be selected. Only the tests for your products/PUT type and speed are shown in the tree based on your inputs from the previous setup step.



4. Next click on the "Configure Tab" to verify proper setup of the application connection points. The SATA Specification Revision 3.20 currently offers two independent test mode for SATA products or products vendors.
    A. Vendor specific test mode – user must have a method of creating the necessary LFTP, MFTP, HFTP, LBP and SSOP test patterns per the above specification, Sections 6.2.4.3 and 6.4.11. This mode would be selected to support BIST-T,A,S mode and will prompt the user for pattern changes when needed to ensure testing with the correct pattern.
    B. Far-end Retimed Loopback (FERL) mode – REQUIRED for all SATA designs per the above specification, Section 6.2.3. Users will need to enable this FERL feature via a BIST Activate (Bidirectional) FIS command set, with the Loopback (L-bit) asserted. In this mode, the Transmit Only (T-bit), Align bypass (A-bit) and Bypass Scrambling (S-bit) are normally all de-asserted, but will be ignored if the L-bit is asserted. In FERL mode, the N4903B or 81134A will be programmed to send the required compliance patterns at the appropriate time, thereby automating the user's products/PUT test solution completely and allowing for simple and quicker test transitions.



5. Next you will see each one of the tests being performed automatically by the application. A running total of completed tests and a summary of pass/failed tests is also provided. When completed you will see a summary of the test results.

6. Click on the "HTML Report" tab to view a more detailed summary of the testing that includes screen shots taken from the scope.

Agilent Technologies

Report Style
Compact Verbose

SATA Test Report

Overall Results: 2 of 9 Tests Failed

Test Configuration Details	
Device Description	
Generation	Gen I
Interface	i
Device Type	Drive
Test Session Details	
Infiniium SW Version	04.21.0000
Infiniium Model Number	DSO81204A
Infiniium Serial Number	No Serial
Last Test Date	10/31/2005 11:20:41 AM

Summary of Results

Margin Thresholds	
Warning	< 2 %
Critical	< 0 %

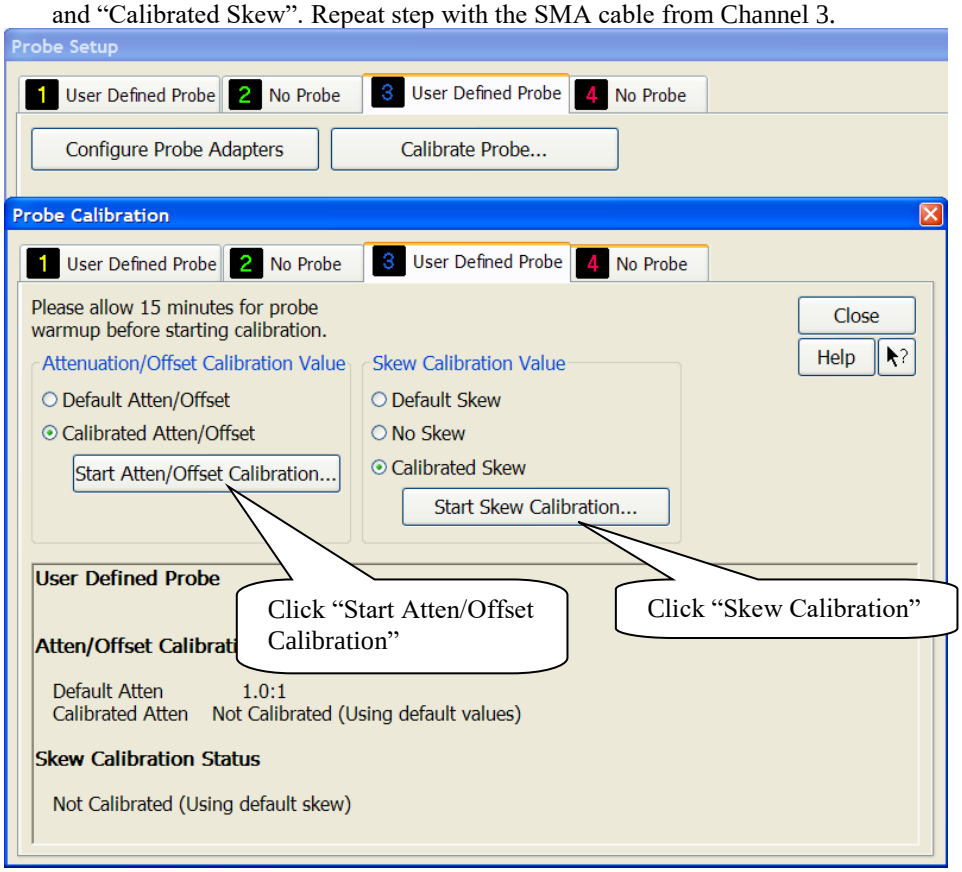
Pass	Test Name	Spec Range	Measured Value	Margin
✓	Channel Speed, FBaud & Unit Interval	[333.2ps to 335.1ps]	333.3ps	5.3 %
✓	TX Risetime	[67.0ps to 136.0ps]	87.3ps	29.4 %
✓	TX Falltime	[67.0ps to 136.0ps]	86.0ps	27.5 %
✗	TX Rise/Fall Imbalance	<= 20.00%	20.76%	-3.8 %
✓	Tx Differential Skew	<= 20.0ps	10ps	50.0 %
✓	TJ at Connector,Clock To Data, fBAUD/500	<= 370mUI	60mUI	83.8 %
✓	DJ at Connector,Clock To Data, fBAUD/500	<= 190mUI	2mUI	100.0 %

Appendix B – Cable Calibration and Deskew Procedure

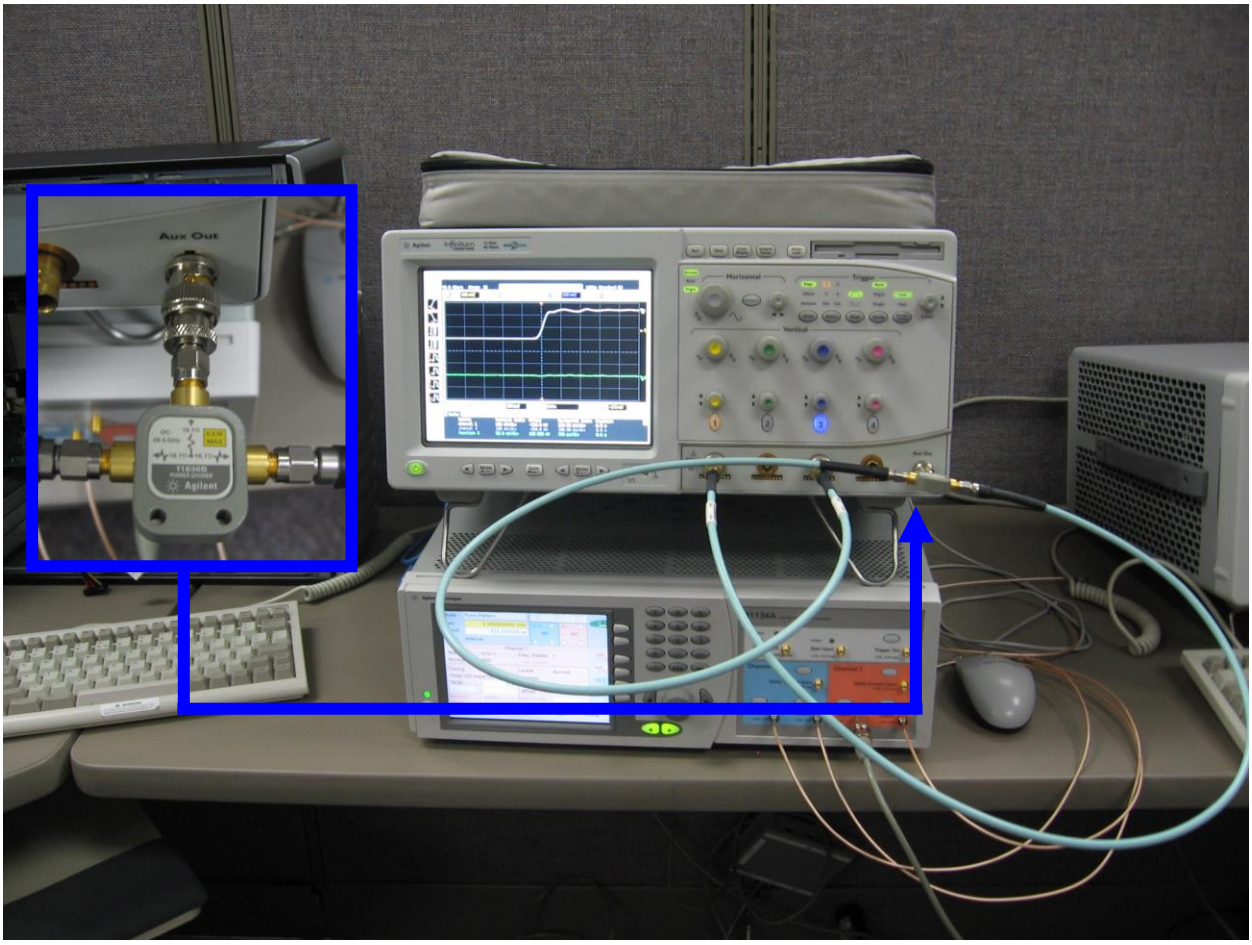
This procedure must be performed before measurements are made, and whenever the skew between the positive and negative data input lines may have changed (i.e. cables have been disconnected and reconnected perhaps on the other side of the diff pair). It is always a good practice to allow any real-time oscilloscope or high-performance electronic instrumentation to warm-up for at least 20 minutes prior to calibrating and deskewing channels to allow all critical input circuitry to achieve a steady state at the ambient operating temperature.

Important note: SMA connectors should always be tightened and removed with a calibrated torque wrench designed for that purpose. The torque wrench should limit torque to 5 inch-pounds.

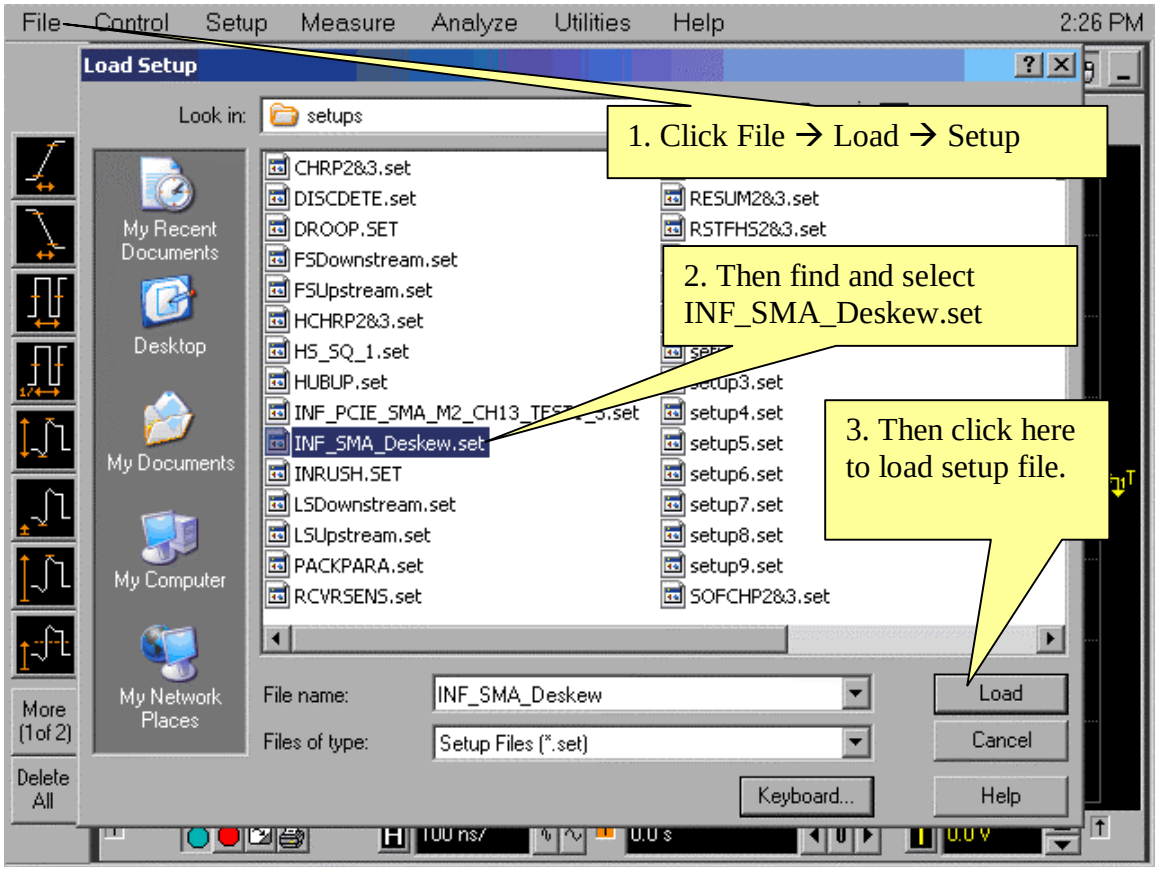
1) Connect one 54855-67604 Precision 7mm (m) to APC 3.5mm (f) adapter each to the inputs of Channel 1 and Channel 3 on the Keysight DSA91204A Infiniium Real-time oscilloscope. These adapters will provide SMA connector compatibility at full bandwidth (13GHz) to the front-end of the oscilloscope.
2) Attach one 36" SMA cable (Rosenberger or equivalent) each to the 54855-67604 adapters on the Channel 1 and Channel 3 inputs of the Infiniium scope. Channel 1 will eventually connect to the products TX+ and Channel 3 to the products TX- outputs.
3) Connect any BNC (m) to SMA (m) adapter to the 'Aux Out' connector on the front panel of the Infiniium scope.
4) For cable and skew calibration, connect the SMA cable from Channel 1 to the 'Aux Out'.
5) On the Probe Setup menu, select "Calibrate Probe". Then, select and start the "Calibrated Atten/Offset" and "Calibrated Skew". Repeat step with the SMA cable from Channel 3.



6) To verify and fine tune the skew calibration, detach the SMA cable from the 'Aux Out' and connect the middle input of the Keysight 11636B Power Divider to the SMA connection on the 'Aux Out' connector adapter, which will split the Aux Out signal source into two phase-matched and amplitude balanced outputs.
7) Now attach the SMA cable outputs from Channels 1 & 3 to the remaining two output connections on the Keysight 11636B Power Divider to complete the deskew connection process.



8) Referring to the figure below, perform the following steps.
   a. Select the **File → Load → Setup** menu to open the Load Setup window.
   b. Navigate to the directory location that contains the **INF_SMA_Deskew.set** setup file.
   c. Select the **INF_SMA_Deskew.set** setup file by clicking on it.
   d. Click the **Load** button to configure the oscilloscope from this setup file.

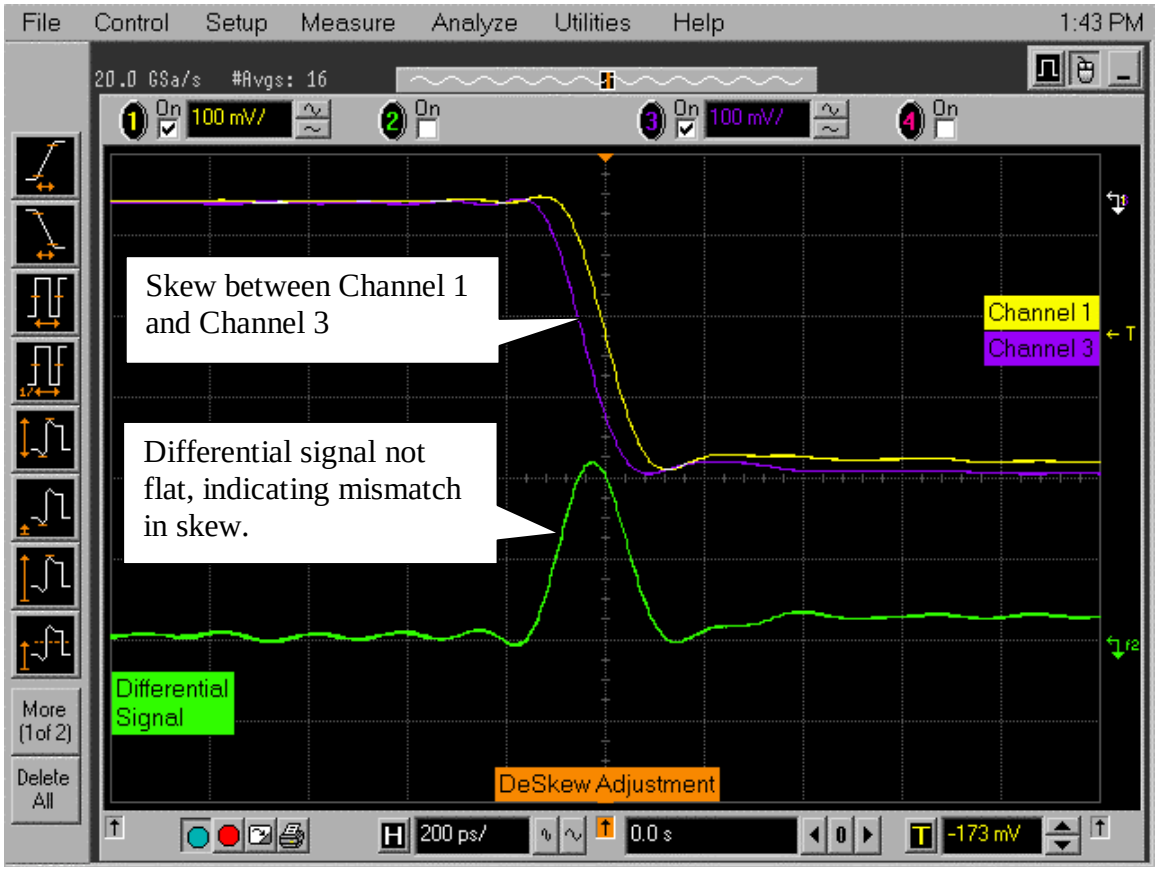


9) If the **INF_SMA_Deskew.set** setup file does not exist, it can be recreated from the following setup configuration on the Infiniium oscilloscope.

INF_SMA_DESKEW.SET setup file details:
Start from a default setup by pressing the **Default Setup** key on the front panel. Then configure the following settings…

Acquisition	Averaging on number of averages 16 Interpolation on
Channel 1	Scale 100.0 mV/ Offset –350mV Coupling DC Impedance 50 Ohms
Channel 3	Turn Channel On; Scale 100.0 mV/ Offset –350m V Coupling DC Impedance 50 Ohms
Time base	Scale 200 ps/sec
Trigger	Trigger level –173mV Slope falling
Function 2	Turn on and configure for channel 1 subtract channel 3, Vertical scale 50 mV/ Offset 100.000 mV

10) The oscilloscope display should look similar to the figure below. A falling edge of the square wave from Aux Out (approximately a 100ps 20%-80% edge) is shown in a 200ps/div horizontal scale. The upper portion of the screen shows channel 1 (yellow trace) and channel 3 (purple trace) superimposed on one another. The lower portion of the screen is the differential signal (green trace) of channel 1 minus channel 3. The top two traces provide for visual inspection of relative time skew between the two channels. The bottom trace provides for visual presentation of unwanted differential mode signal resulting from relative channel skew.



11) Referring to the following figure, perform the following steps to deskew the channels.
    a. Click on the **Setup → Channel 1** menu to open the **Channel Setup** window.
    b. Move the **Channel Setup** window to the left so you can see the traces.
    c. Adjust the Skew by clicking on the ← or → arrows, to achieve the flattest response on the differential signal (green trace).
    d. Click the **Close** button on the Channel Setup window to close it.
    e. The de-skew operation is complete.
    f. Disconnect the cables from the Tee on the Aux Out BNC. Leave the cables connected to the Channel 1 and Channel 3 inputs.

NOTE: Each cable is now deskewed for the oscilloscope channel it is connected to. Do not switch cables between channels or other oscilloscopes, or it will be necessary to deskew them again. It is recommended that the cables be labeled with the channel they were calibrated for.

12) The figure below shows the desired effect of no skew between the cables. Note that the channel 1 (yellow trace) & channel 3 (purple trace) traces overlap, and the differential signal (green trace) is flat. If this is not the case, then repeat the steps in section 8 above.

Appendix C – Verification of Lab Load Return Loss

Purpose: To provide verification that the measurement instrument meets the Lab Load requirement of the SATA spec.

References: [1] Serial ATA Revision 3.0, 7.2.2.4 *Lab Load Details*

Last Modification: March 25, 2009 (Revision 1.65)

Discussion:

C.1 - Introduction

The Serial ATA Revision 3.0 specifies a requirement for the 'Lab Load', which is defined in [1] as the fixture (not including the SATA connector), cables, DC blocks, and the 50 ohm terminations inside of the HBWS. Measurement of the setup as specified requires destructive modification to the SATA test fixture, which would not be representative of interoperability conditions during conformance testing described in [2]. Therefore, a reasonable approximation to this measurement is to verify the return loss of the instrument, cables and DC blocks used to perform the measurement (as this is the dominant source of potential reflections due to impedance mismatch, provided high-quality cables and components are used.)

In this measurement, the return loss of an Keysight DSA91204A Real-Time DSO was measured, using an Keysight 86100C DCA-J Digital Communications Analyzer with a 54754A 18GHz Differential TDR module. The DSO was set to 50mv/div vertical resolution, and was actively sampling at 40GS/s during the measurement. The 86100C was set to measure from DC to 20GHz. For documentation and verification purposes, two separate calibrations were made and two separate measurements performed to validate both the S11 and S22 single-ended return loss of Channels 1 and 3 of the DSO81304B, as well as the SDD11 differential return loss of the same channels, respectively. This is done to provide full coverage of any interpretation of the lab load requirement as stated in [1], either single-ended or differential. The results of both measurement studies are provided in C.2 below.

The setup for the 86100C and 54754A includes a full frame and module calibration using standard SMA shorts and loads. The vertical scale for channels 1 and 2 is set to 100mV/div and the timebase set to 2.00ns/div, to ensure that the entire length of the laboratory load is included in the TDR pulse response on the 86100C. The TDR stimulus edge rate is set to 35ps. Option 202 Enhanced Impedance and S-Parameters measurement software provides the conversion between the time-domain TDR response and the frequency domain return loss plots. Note: for single-ended return loss measurements, the TDR Stimulus Mode is set to Single-Ended (see Figure C.1a); for differential return loss measurements, the TDR Stimulus Mode is set to Differential (see Figure C.1b).

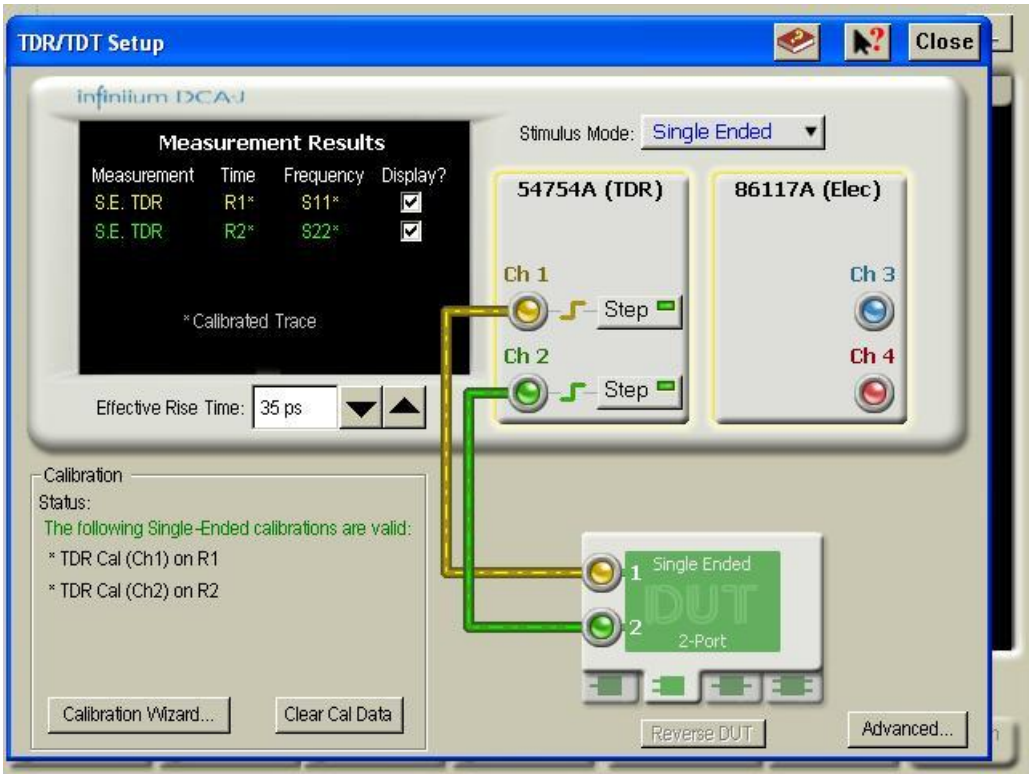


Figure C.1a TDR Single-ended stimulus setup for Keysight 86100C DCA-J

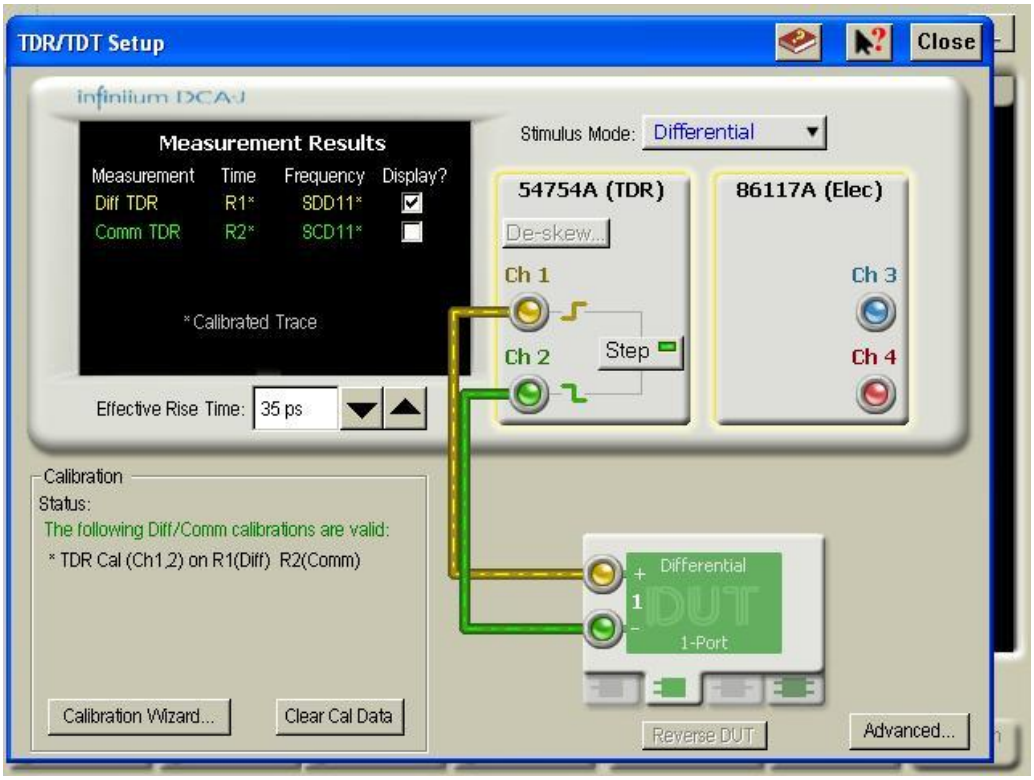


Figure C.1b TDR Differential stimulus setup for Keysight 86100C DCA-J

C.2 – Measurement Results

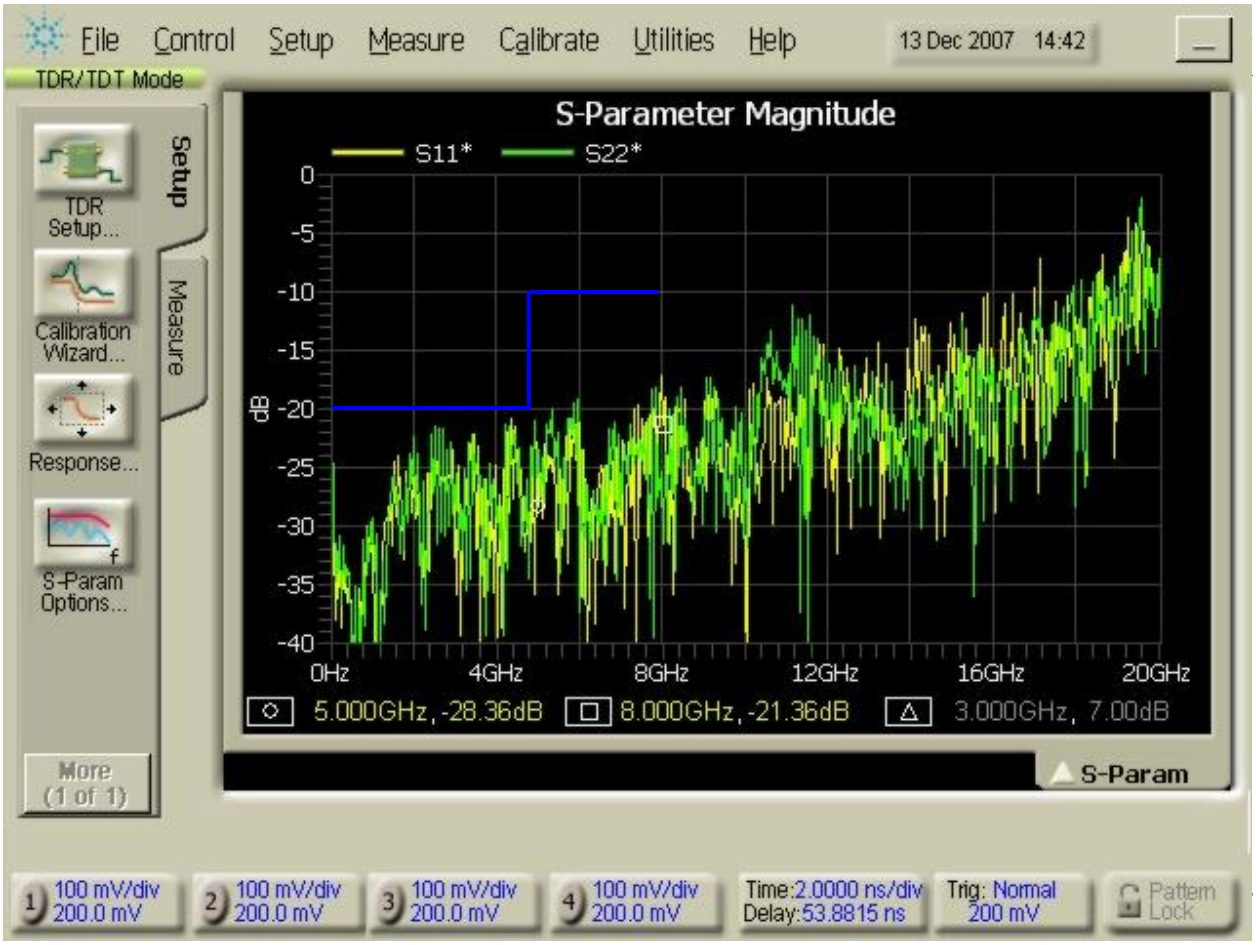


Figure C.2a Differential return loss measurement for Keysight's DSA91204A laboratory load (including Rosenberger SMA cables and 11742A DC blocking capacitors)

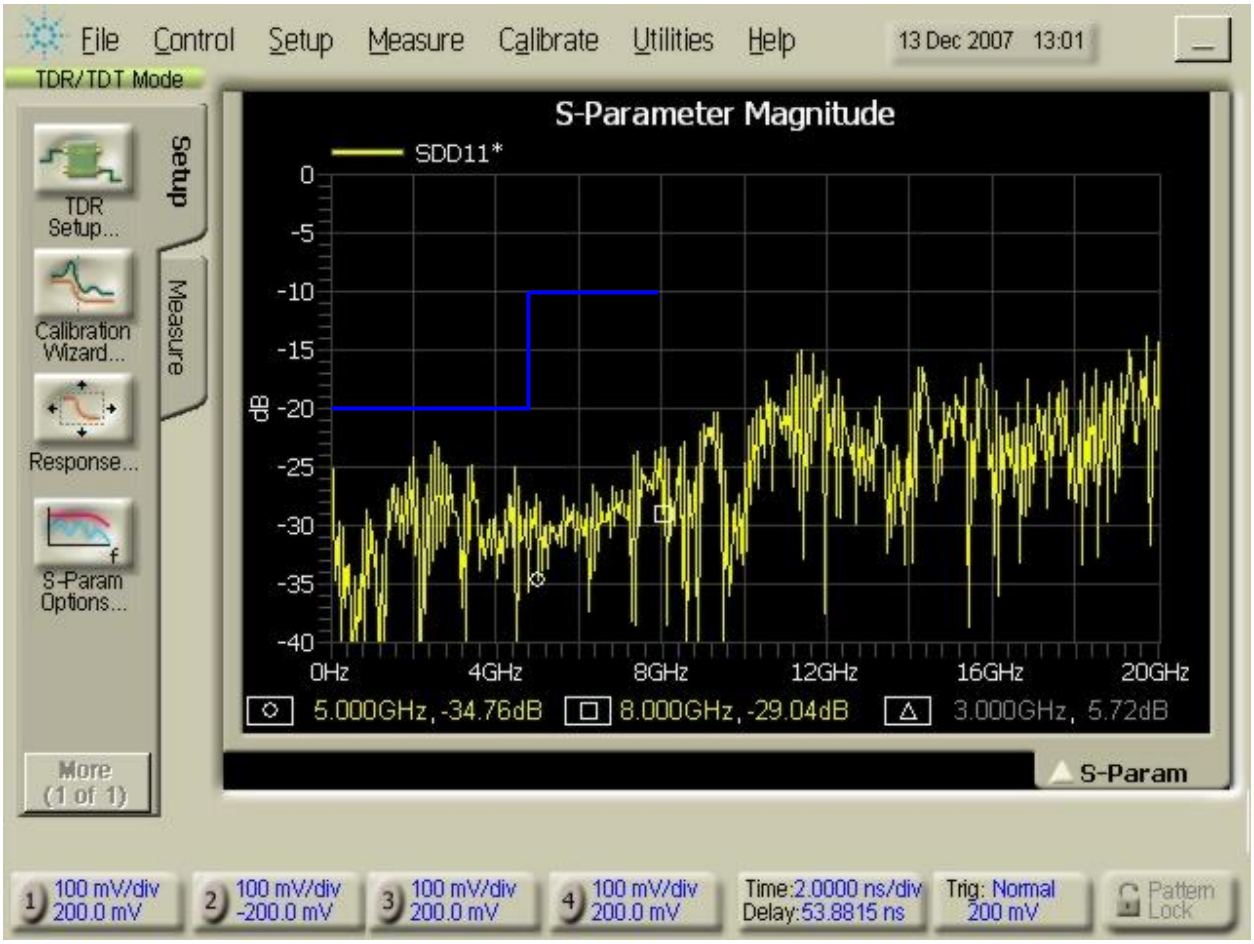


Figure C.2b Differential return loss measurement for Keysight's DSO81304B laboratory load (including Rosenberger SMA cables and 11742A DC blocking capacitors)

Appendix D - Measurement Accuracy Specifications

Measurement:	Accuracy:	Accuracy Source:
PHY-01 UI	1.2 ps rms	MFTP Measured
PHY-02 Long Term Freq	+/- 1ppm	Data Sheet
PHY-03 SSC Freq	+/- 1ppm	Data Sheet
PHY-04 SSC Dev	+/- 1ppm	Data Sheet
TSG-01 Dif Out Volt	2.71mV at 800mVFull Screen	Data Sheet
TSG-02 Rise Fall Time	<1ps rms	
TSG-03 Skew	<100fs rms	MFTP with 1UI offset Measured
TSG-04 AC Com Mode	<2mV rms at 800mV Full Screen	MFTP with 1UI offset Filtered and Measured
TSG-05 Rise Fall Imb	<1.5%	Fast Edge against inverted signal Measured
TSG-06 Amp Imb	<0.5%	MFTP Measured
TSG-07 Tj	800fs rms	Data Sheet
TSG-08 Dj	800fs rms	Data Sheet
TSG-09 Tj	800fs rms	Data Sheet
TSG-10 Dj	800fs rms	Data Sheet
TSG-11 Tj	800fs rms	Data Sheet
TSG-12 Dj	800fs rms	Data Sheet

Appendix E – Calibration of Jitter Measurement Devices

Purpose: To calibrate and verify the jitter measurement device (JMD) and associated test setup has a proper response to jitter and SSC.

References:

[1] SATA Specification Revision 3.0, Section 7.3.2

Resource requirements:

Pattern Generator for SATA signals
Sine wave source, 30kHz, and 0.5MHz to 50MHz.
Test cables
Jitter Measuring Device

Last Template Modification:

May 3, 2013 (Version 1.65)

Discussion:

See Reference [1].

Test Procedure:

The response to jitter of the Jitter Measurement Device (JMD)(the reference clock is part of the JMD) is measured with three different jitter modulation frequencies corresponding to the three cases: 1) SSC (full tracking) 2) jitter (no tracking) 3) the boundary between SSC and jitter. The jitter source is independently verified by separate means. This ensures the jitter response of the JMD is reproducible across different test setups.

The three Gen1i test signals are: 1) a 375MHz +/- 0.035% square wave (which is a D24.3, 00110011 pattern) with risetime between 67ps and 136ps 20 to 80% [1] with a sinusoidal phase modulation of 20.8ns +/- 10% peak to peak at 30kHz +/- 1%. 2) a 375MHz square wave with a sinusoidal phase modulation of 200ps +/- 10% peak to peak at 50MHz +/- 1%. 3) a 375MHz square wave with no modulation.

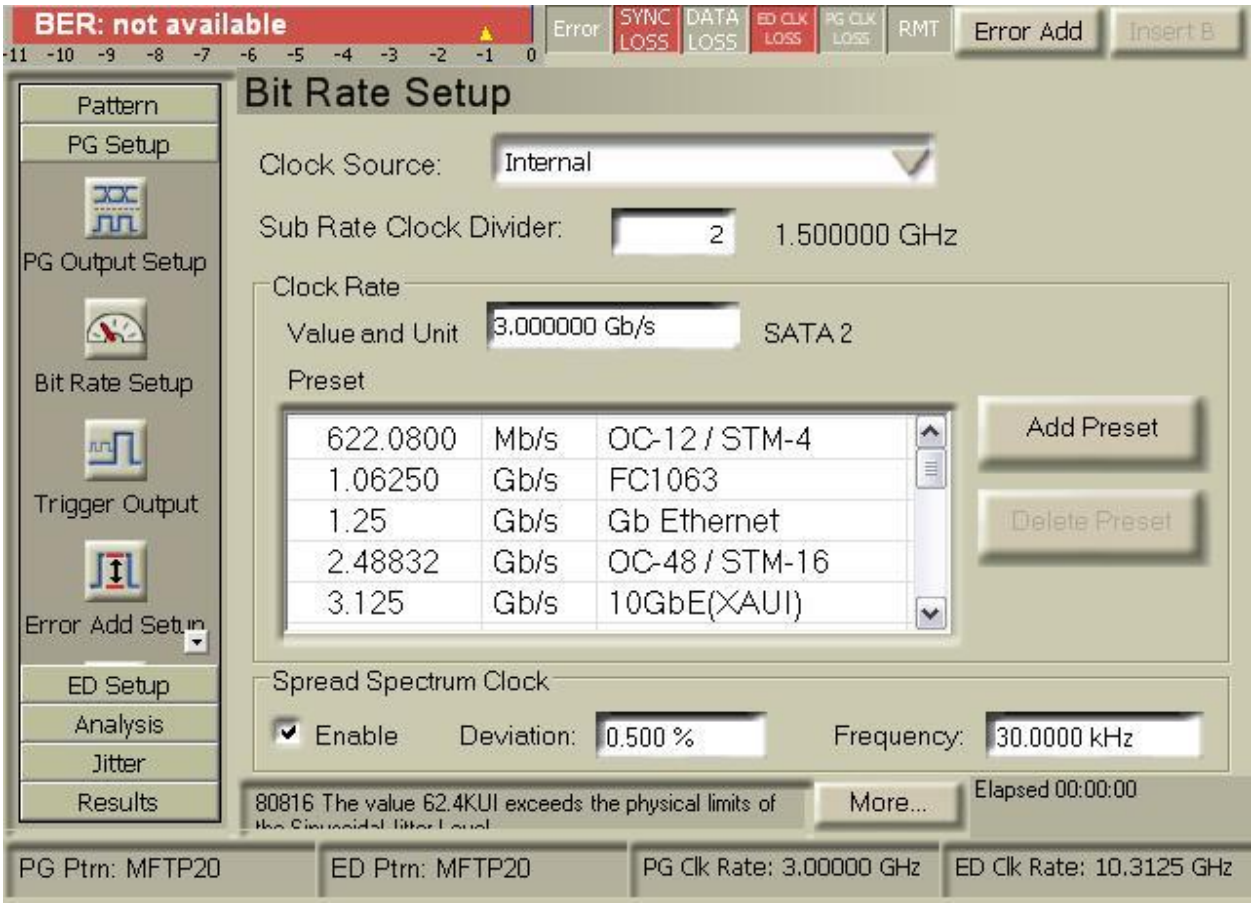
The three Gen2i test signals are: 1) a 750MHz +/- 0.035% square wave (which is a D24.3, 00110011 pattern) with risetime between 67ps and 136ps 20 to 80% [1] with a sinusoidal phase modulation of 20.8ns +/- 10% peak to peak at 30kHz +/- 1%. 2) a 750MHz square wave with a sinusoidal phase modulation of 100ps +/- 10% peak to peak at 50MHz +/- 1%. 3) a 750MHz square wave with no modulation.

The three Gen3i test signals are: 1) a 1500MHz +/- 0.035% square wave (which is a D24.3, 00110011 pattern) with risetime between 33ps and 67ps (20 to 80%) [1] with a sinusoidal phase modulation of 1.0ns +/- 10% peak to peak at 420kHz +/- 1%. 2) a 1500MHz square wave with a sinusoidal phase modulation of 50ps +/- 10% peak to peak at 50MHz +/- 1%. 3) a 1500MHz square wave with no modulation.

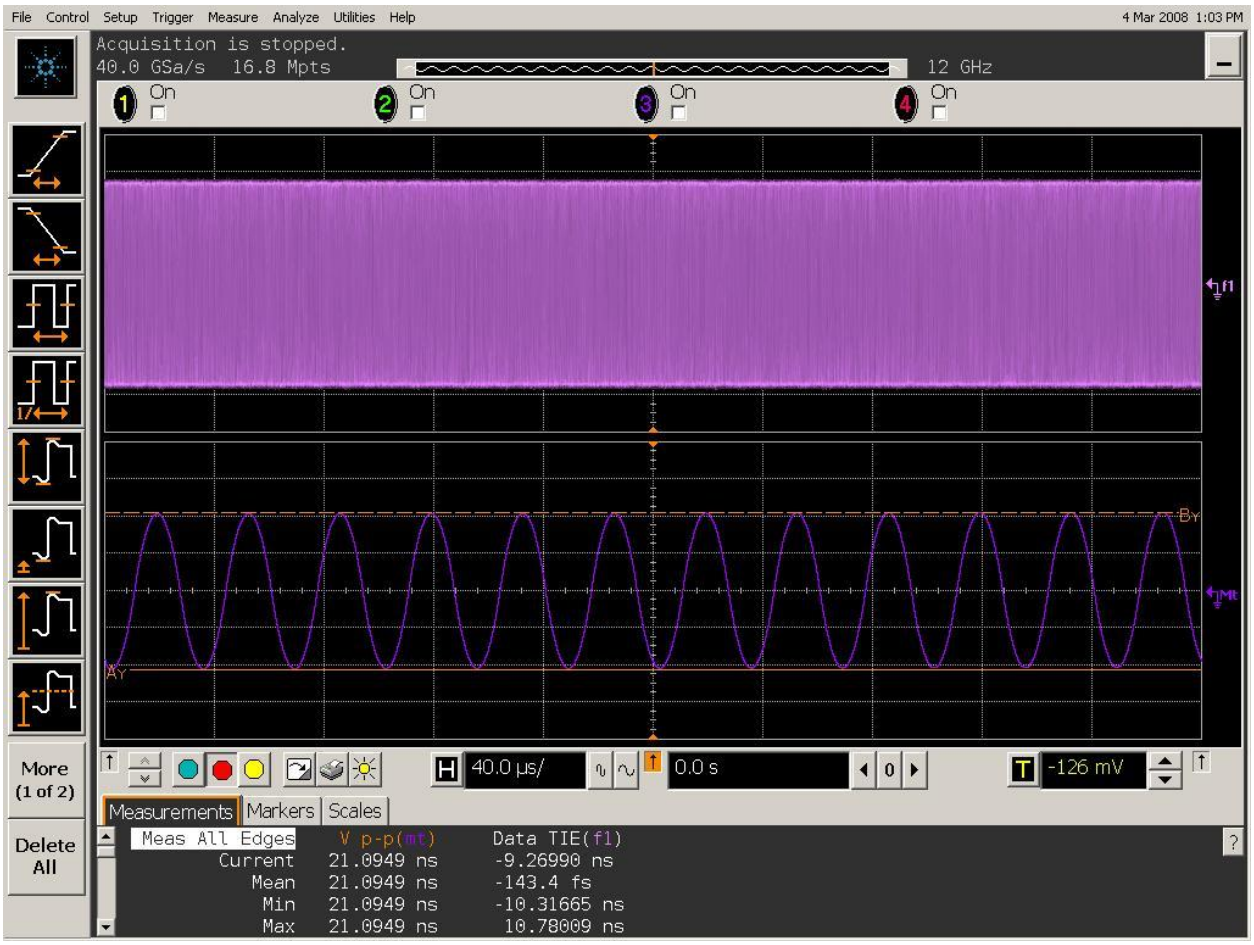
An independent separate means of verification of the test signals is used to make sure the level of the modulation is correct.

The test procedure checks two conditions: the JTF attenuation and the JTF bandwidth. Care is taken to minimize the number of absolute measurements taken, making most relative; this reduces the dependencies and improves accuracy.

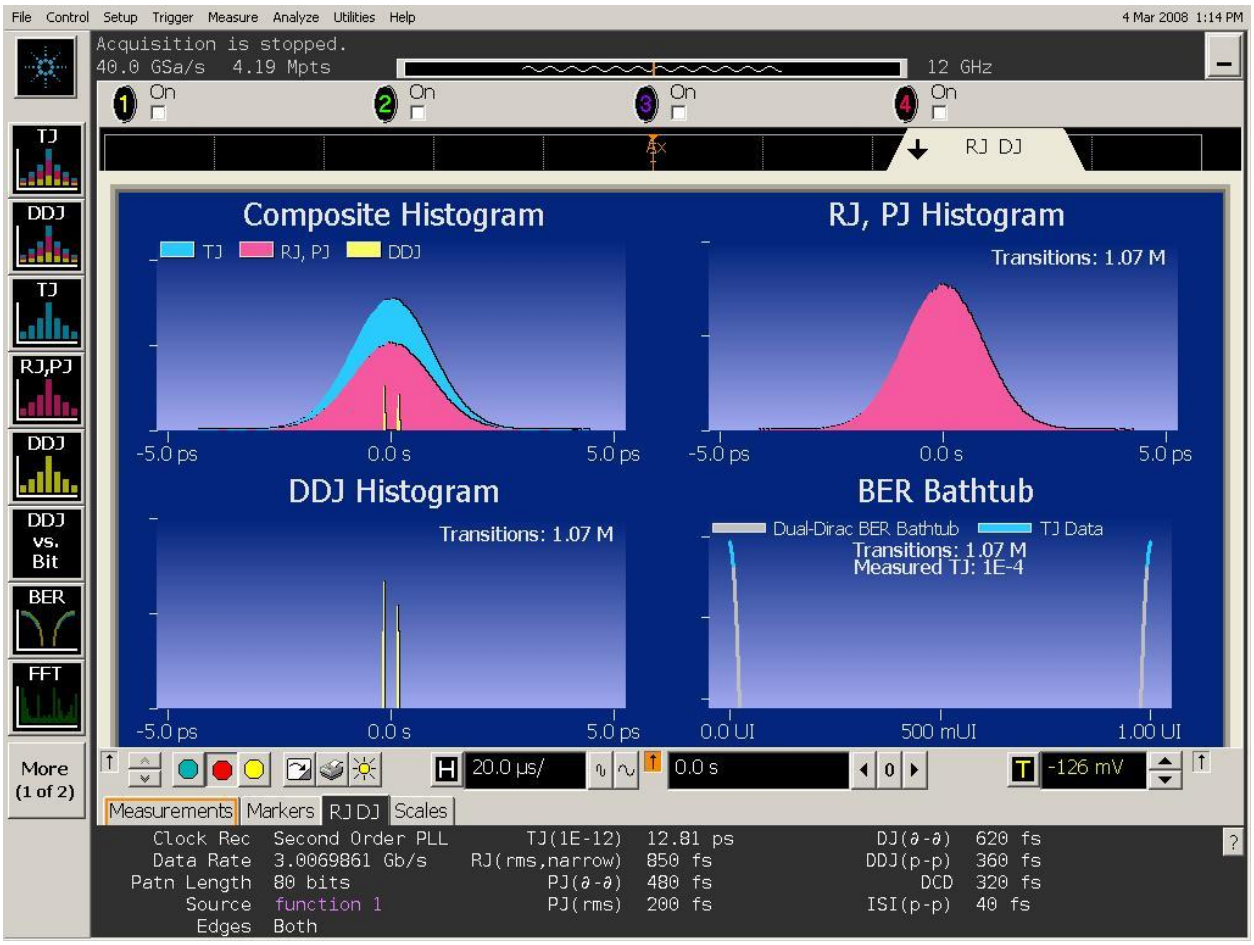
1. For Gen1 and Gen 2 calibration, adjust the pattern generator for a D24.3 pattern (00110011, with a risetime within specified limits) modulation to produce a 30 KHz +/- 1%, 20.8 ns p-p +/- 10% sinusoidal phase modulation. For Gen 3 calibration, adjust the pattern generator for a D24.3 pattern (00110011, with a risetime within specified limits) modulation to produce a 420kHz +/- 1%, 1.0 ns p-p +/- 10% sinusoidal phase modulation.


BER: not available
-11 -10 -9 -8 -7 -6 -5 -4 -3 -2 -1 0
Error
SYNC LOSS
DATA LOSS
ED CLK LOSS
PG CLK LOSS
RMT
Error Add
Insert E
Pattern
PG Setup
PG Output Setup
Bit Rate Setup
Trigger Output
Error Add Setup
ED Setup
Analysis
Jitter
Results
Bit Rate Setup
Clock Source:
Internal
Sub Rate Clock Divider:
2
1.500000 GHz
Clock Rate
Value and Unit
3.000000 Gb/s
SATA 2
Preset
622.0800 Mb/s OC-12 / STM-4
1.06250 Gb/s FC1063
1.25 Gb/s Gb Ethernet
2.48832 Gb/s OC-48 / STM-16
3.125 Gb/s 10GbE(XAUI)
Add Preset
Delete Preset
Spread Spectrum Clock
Enable
Deviation:
0.500 %
Frequency:
30.0000 kHz
80816 The value 62.4KUI exceeds the physical limits of
More...
Elapsed 00:00:00
PG Ptrn: MFTP20
ED Ptrn: MFTP20
PG Clk Rate: 3.00000 GHz
ED Clk Rate: 10.3125 GHz

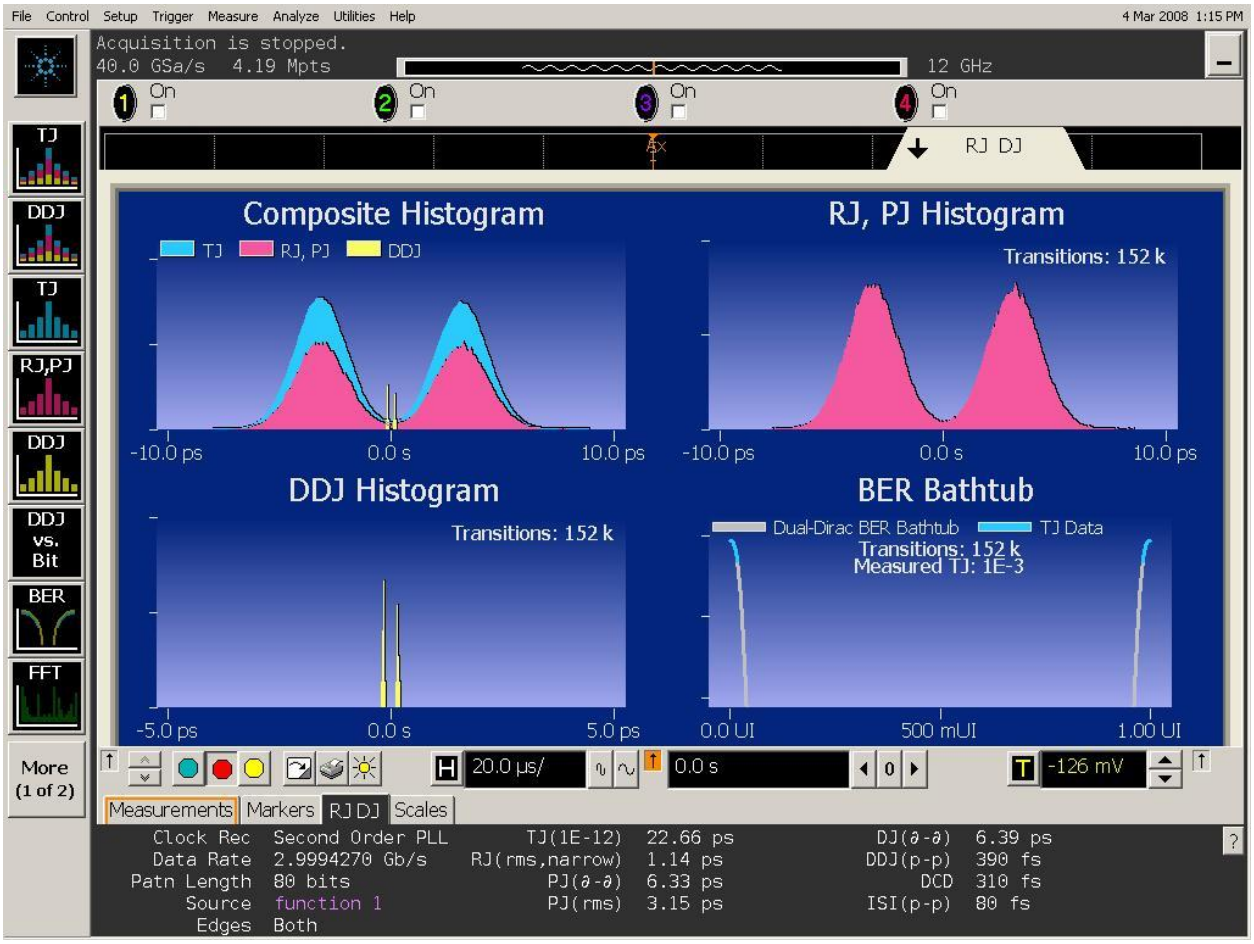
2. Verify the level of modulation meets the requirements and record the p-p level, **DJSSC**. This is done with a Time Interval Error (TIE) type measurement or equivalent.



3. Apply test signal to the JMD. Turn off the sinusoidal phase modulation. Record the reported DJ, **DJSSCOFF**.

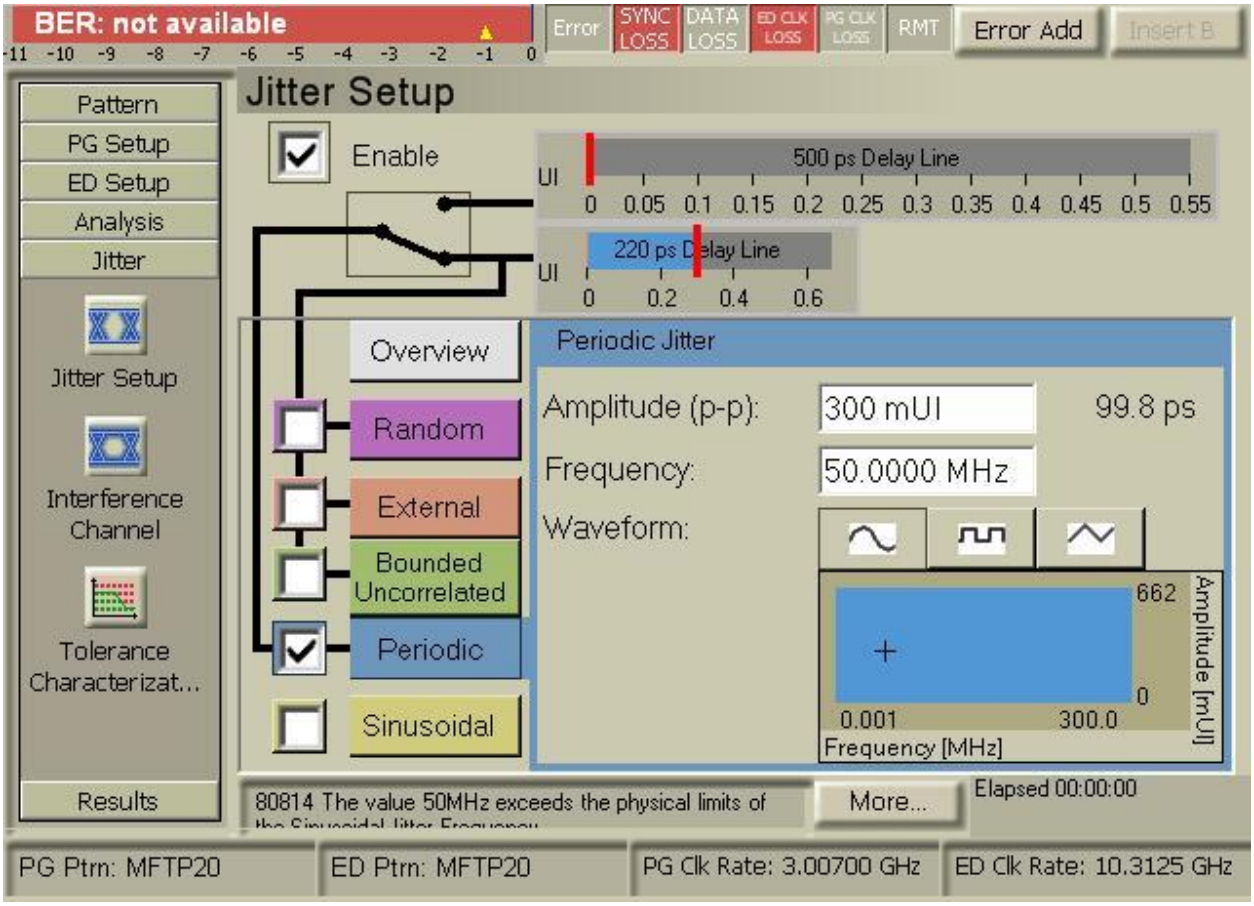


4. Turn on the sinusoidal phase modulation. Record the reported DJ, **DJSSCON**.

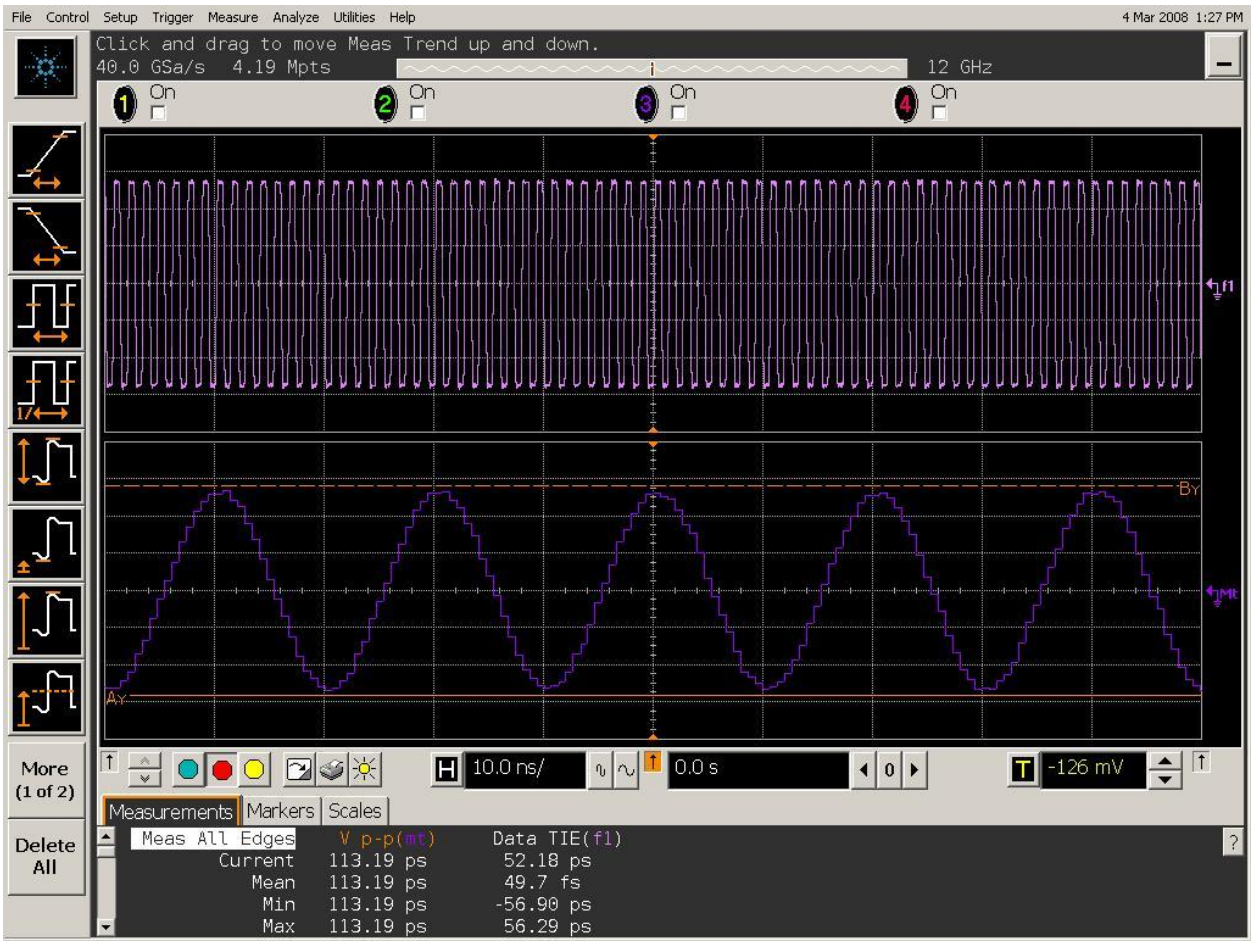


5. Calculate and record the level of measured DJ by subtracting the DJ with modulation off from DJ with modulation on, **DJMSSC = DJSSCON - DJSSCOFF**. Calculate the jitter attenuation by 20Log(**DJMSSC** / **DJSSC**). This value must fall within the range of –72dB +/- 3dB for Gen1 or Gen 2. The value must fall within the range of -38.2dB +/-3dB for Gen3. Adjust the JMD settings to match this requirement.

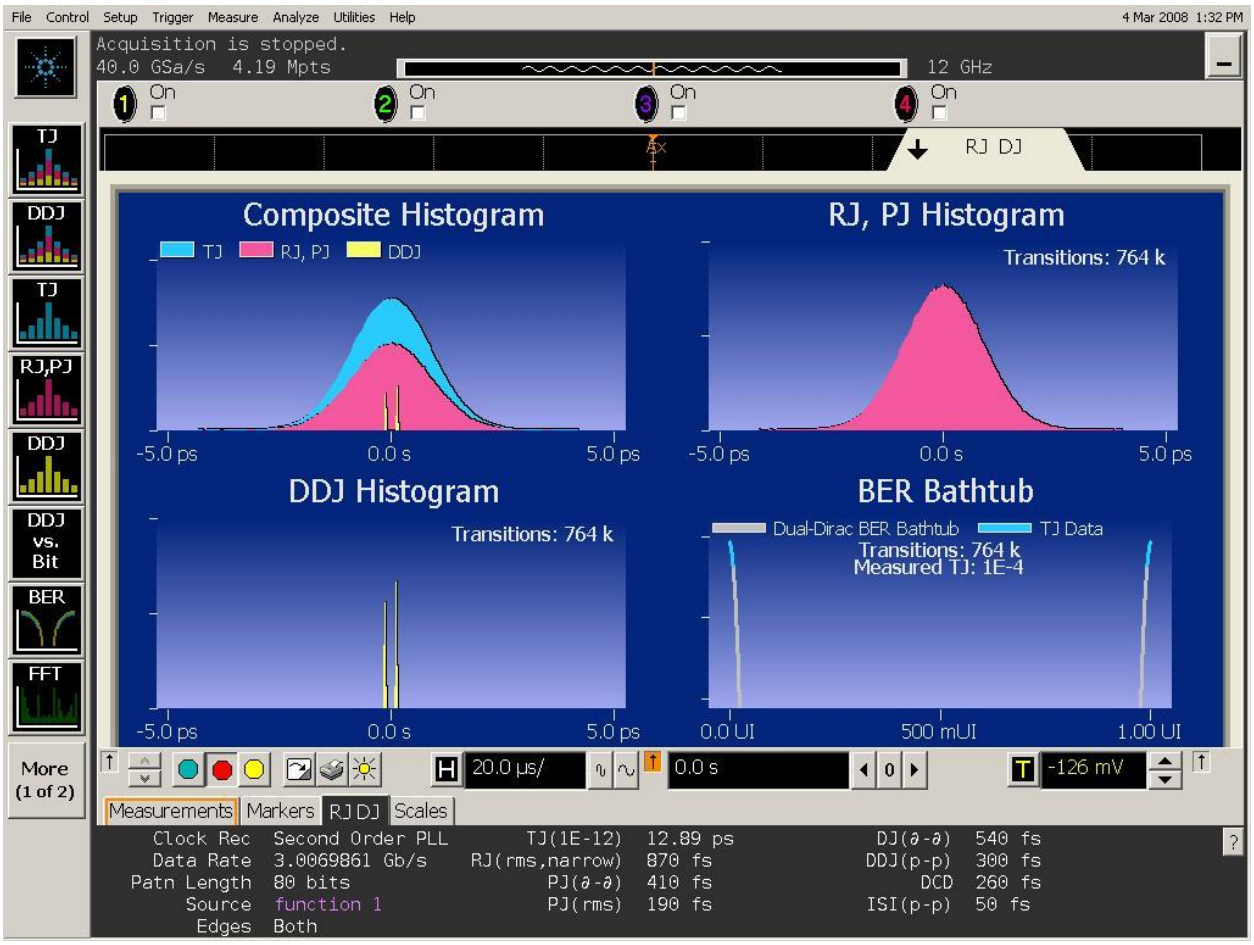
6. Adjust the pattern generator for a D24.3 pattern (00110011) and modulation to produce a 50 MHz +/-1%, 0.3 UI p-p +/- 10% (200ps for Gen1i or 100ps for Gen2i or 50ps for Gen3i) sinusoidal phase modulation, also known as periodic jitter, PJ.



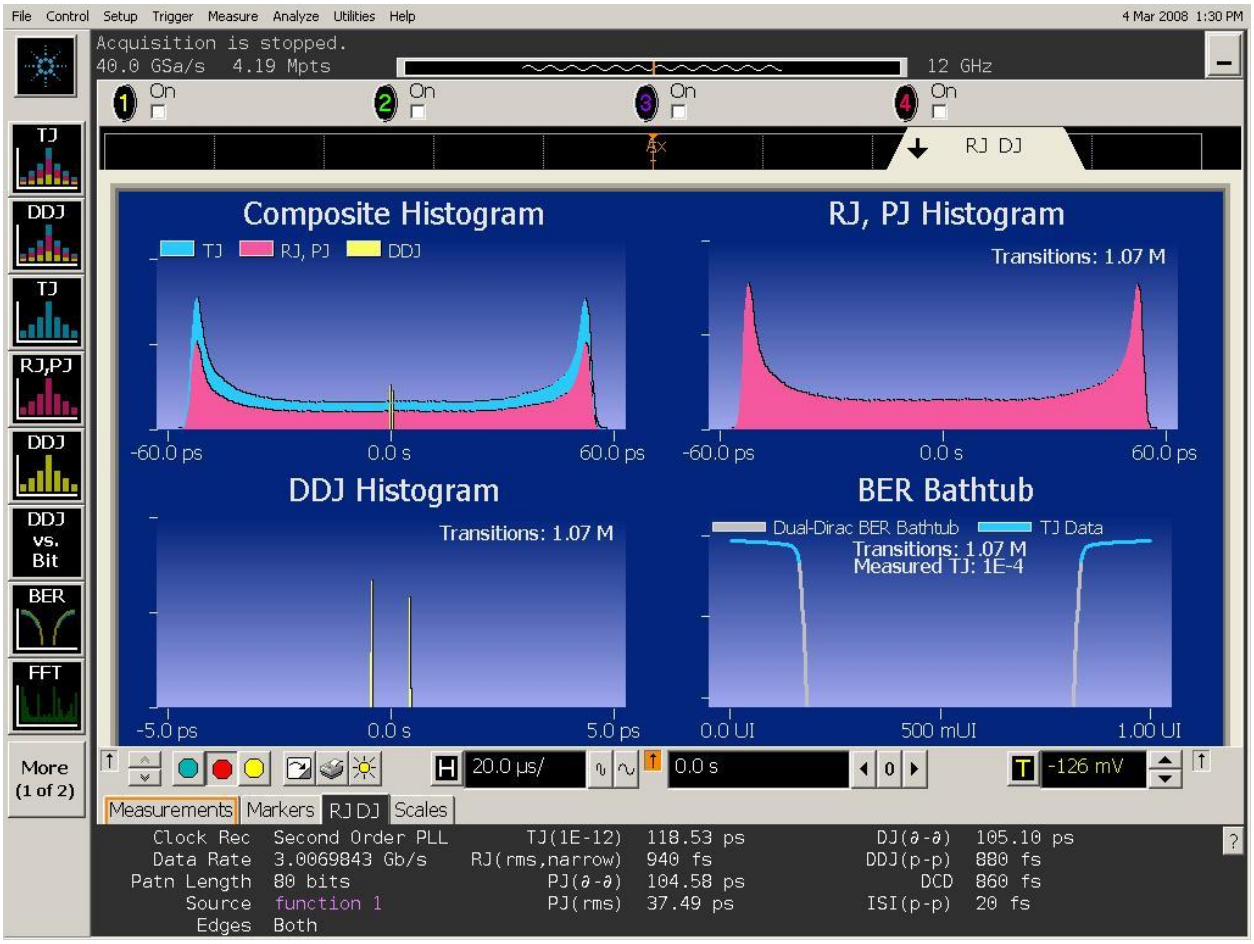
7. Verify the level of modulation meets the requirements and record the p-p level, **DJM.** This is done with a Time Interval Error (TIE) type measurement or equivalent.



8. Apply test signal to the JMD. Turn off the sinusoidal phase modulation. Record the reported DJ, **DJMOFF**.

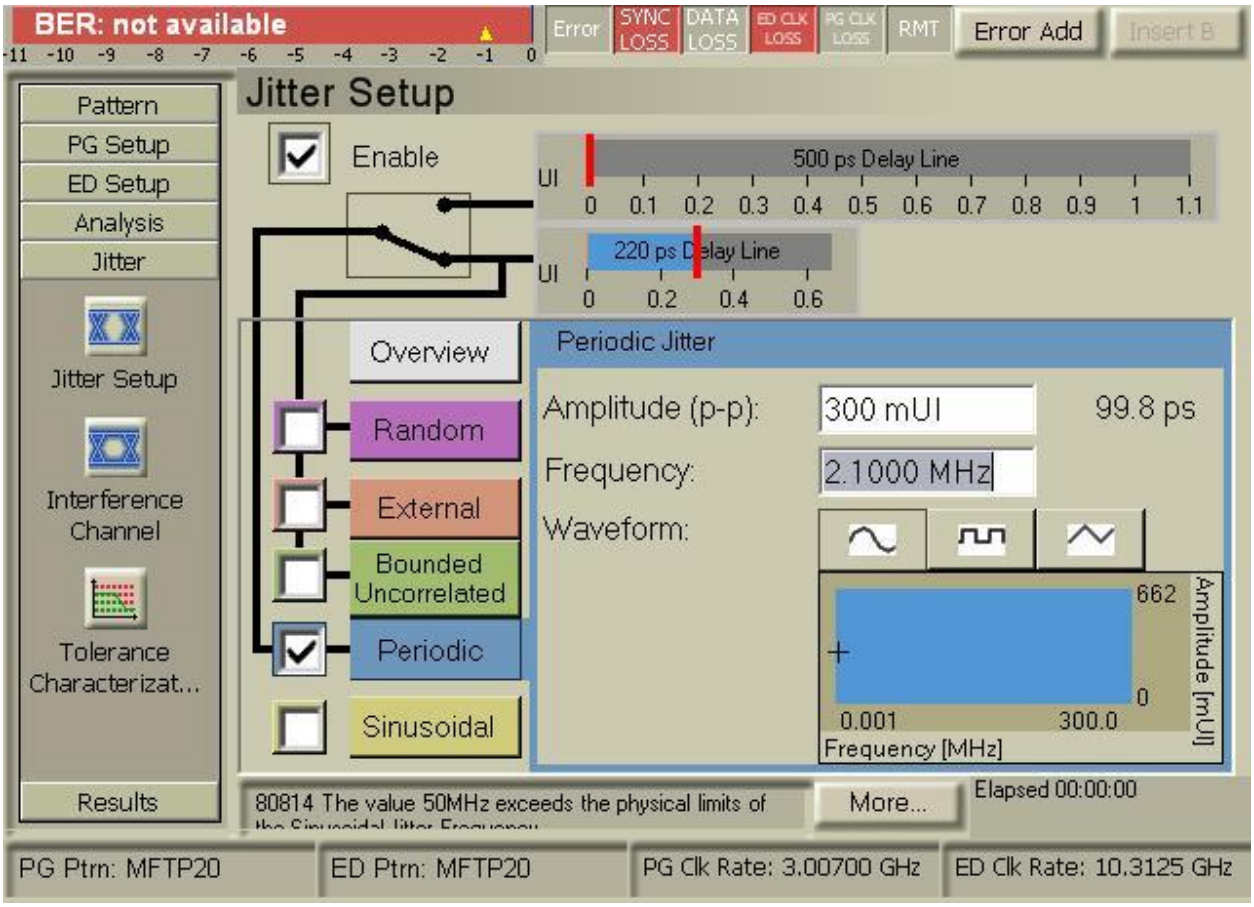


9. Turn on the sinusoidal phase modulation. Record the reported DJ, **DJMON**.

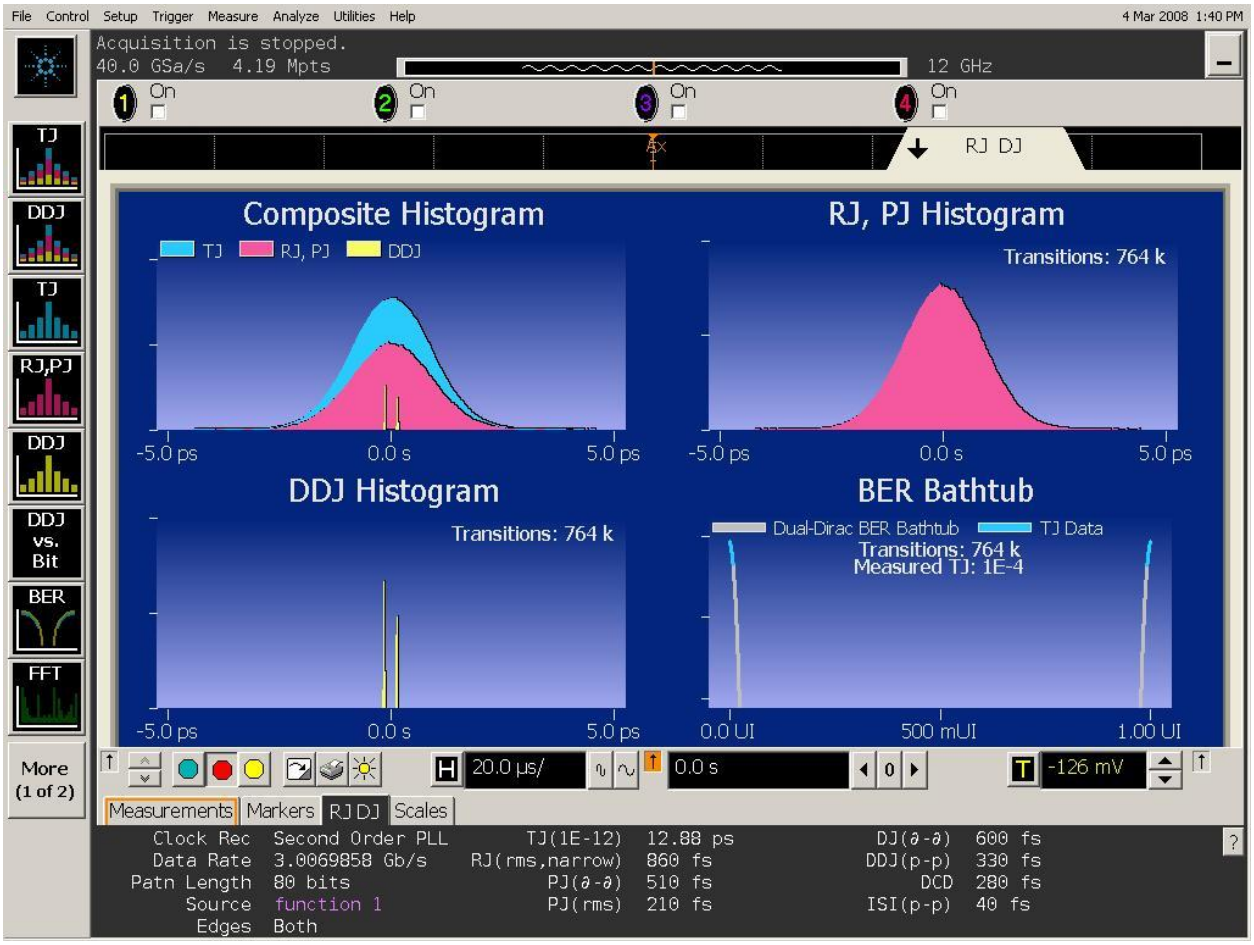


10. Calculate the difference in reported DJ for these two cases, **DJMM = DJMON - DJMOFF** Calculate the -3dB value: **DJ3DB** = **DJMM** * 0.707

11. Adjust the frequency of the PJ source to 2.1MHz for Gen1 or Gen2 calibration, 4.2MHz for Gen3 calibration

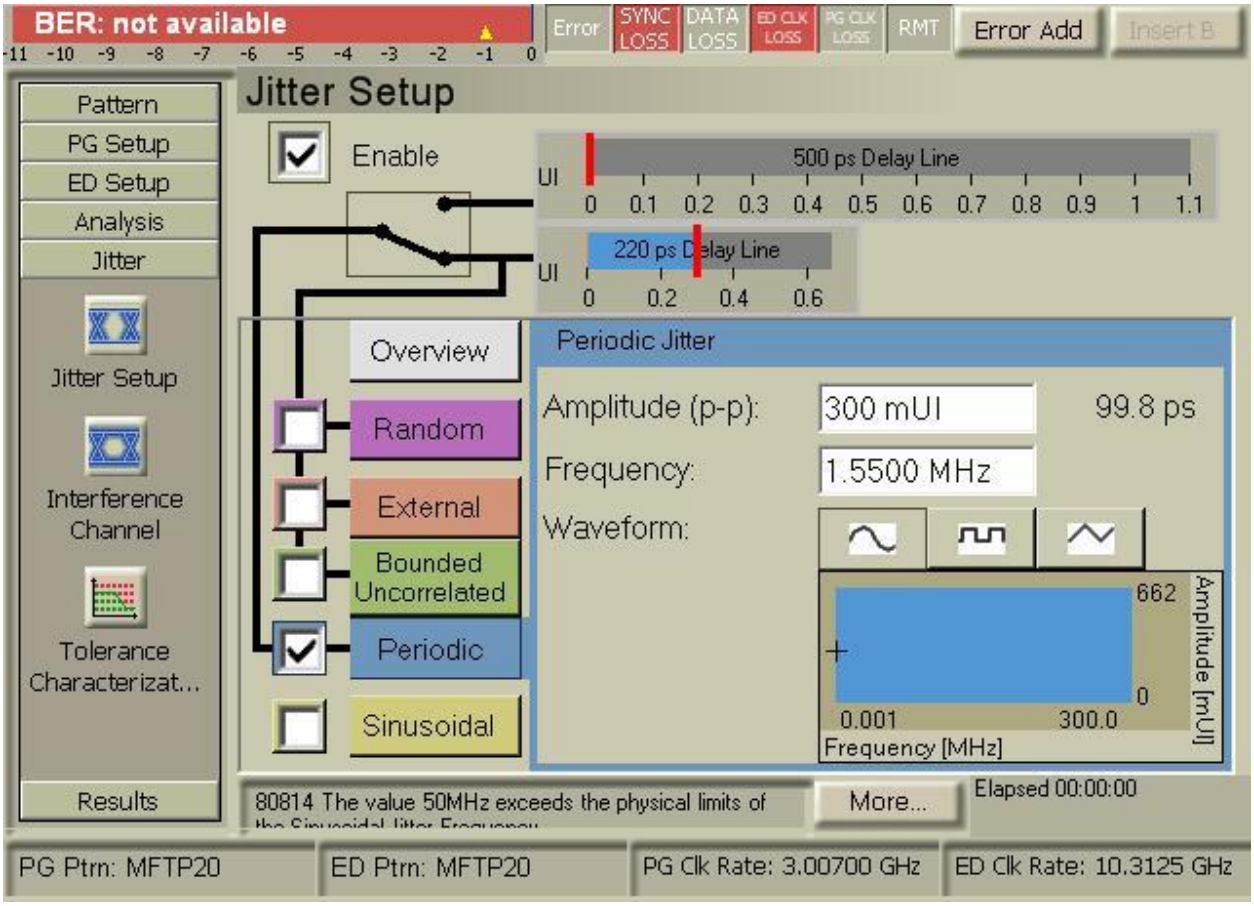


12. Measure the reported DJ difference between PJ on versus PJ off **DJ = DJON - DJOFF** and compare to the (DJ -3dB) value, **DJ3DB**. Shift the frequency of the PJ source until the reported DJ difference between PJ on versus PJ off is equal to (DJ -3dB). The PJ frequency is the -3dB BW of the JTF; record this value **F3DB**.



13. Adjust the JMD settings to bring the PJ –3dB frequency to 2.1MHz +/- 1MHz for Gen1 or Gen2 calibration, 4.2MHz +/- 1MHz for Gen3 calibration. Repeat steps 4 through 12 until both the jitter attenuation and 3dB frequency are in the acceptable ranges.
    a. For Keysight's DSAX93204A, DSAX92804A, DSAX92504A, DSAX92004A and DSAX91604A and DSA91204A Infiniium Oscillocope, the clock recovery settings used to achieve the JTF calibration requirements are:
    Gen 1: 2nd order PLL, Loop Bandwidth = 2.10 MHz, Damping Factor = 0.767
    Gen 2: 2nd order PLL, Loop Bandwidth = 2.10 MHz, Damping Factor = 0.767
    Gen 3: 2nd order PLL, Loop Bandwidth = 4.20 MHz, Damping Factor = 0.767
    b. These settings meet the JTF calibration requirements at all data rates
    c. These settings are the same for the DSO81304A Infiniium Oscilloscope

14. Check the peaking of the JTF. Adjust the pattern generator for a D24.3 pattern and modulation to produce sinusoidal phase modulation (PJ) at the –3dB BW frequency found above, and 0.3 UI p-p +/- 10% (200ps for Gen1i or 100ps for Gen2i or 50ps for Gen3i). Increase the frequency of the modulation to find the maximum reported DJ; it is not necessary to increase beyond 20MHz. Measure the reported DJ difference between PJ on versus PJ off, **DJPK = DJPKON - DJPKOFF**. Record this DJ difference (**DJPK**) and frequency, **F3PK**.



15. Calculate the JTF Peaking value: 20Log (**DJPK / DJMM**). Record this value.

Worksheet Results Example for Gen1/2 JTF Calibration

	Recorded Values		Calculated Values		Calculated Values
DJSSC, applied PM at 30kHz	2.15E-08				
DJSSCON, measured jitter at 30kHz	6.20E-12				
DJSSCOFF, measured residual jitter at 30kHz	6.20E-13	**DJMSSC**	5.58E-12	**Attenuation**	-71.716085
DJM, applied jitter at 50MHz	1.13E-10				
DJMON, measured jitter at 50MHz	1.05E-10				
DJMOFF, measured residual jitter at 50MHz	5.40E-13	**DJMM**	1.045E-10	**DJ3DB**	7.3853E-11
DJON, measured jitter at 3dB point	7.42E-11				
DJOFF, measured residual jitter at 3dB point	6.00E-13	**DJ**	7.36E-11		
F3DB, 3dB frequency	1.55 MHz				
DJPKON, measured jitter at peaking frequency	1.06E-10				
DJPKOFF, measured residual jitter at peaking frequency	6.00E-13	**DJPK**	1.053E-10	**Peaking**	3.10771103
FPK, peaking frequency	16 MHz				